Analysis and design of a voltage unbalance controller for single-phase half-bridge AC-AC converter

M. T. Tsai, Professor J. H. Wu, Student

Department of Electrical Engineering, Southern Taiwan University

Abstract

A single-phase AC-AC converter for source voltage regulation applications is considered. An improved control algorithm to balance the two split dc bus voltages is proposed. The new idea is to use a PI controller instead of the conventional P controller. It shows the new strategy can further improve the voltage unbalance quantity between the two split dc bus. Theoretical analysis has been achieved, and DSP TMS320LF2407A based case studies have demonstrated the effectiveness and performance of this converter.

Keywords: AC-AC, half-bridge, balance.

I Introduction

Voltage-sensitive equipment requires a well regulated load voltage to withstand the source voltage deviation, which can cause severe process disruptions and result in production loss. An ac voltage regulator (AVR) can provide a well regulated voltage source, and is becoming more and more important due to the rapid decrease in the quality of power systems [1-7]. A number of converter topologies such as full-bridge and half-bridge configurations have been reported. Among them, the half-bridge topology presents an interest as it has a small size, and requires a relatively little number of power switches [1-4]. However, it is worth to highlight the dc bus voltage unbalance problem in accordance with this topology. The unbalance voltages may be resulted by the small dc variation in the circuit components and controllers, or the load characteristic. To ensure both the positive and negative sides of dc buses to be equal, a balance loop which sensing the error of the two dc bus voltages, and subtracting it from the command current has been proposed by other authors [1-2], and is widely used in this structure. However, based on the following analysis, one can see that the compensation algorithm is still containing a dc bias between the two split bus voltages, and a further improvement is necessary.

This paper proposes a new compensation algorithm to further reduce the dc bias unbalance. The explanation for unbalance phenomenon has been given in the following section, and a 1 kVA prototype is examined to verify the proposed control idea.

II. System analysis

Fig. 1 shows the considering single-phase half-bridge AVR. It consists of an ac-dc topology, and a dc-ac topology. From Fig. 1, the following equations can be obtained, where D_1 and D_2 are related to the duty cycles of Q_1 and Q_2:

$$i_{Q1} = i_S D_1, \quad i_{Q2} = i_L D_2 \tag{1}$$

$$C_1\frac{dV_1}{dt} = -i_{Q1} + i_{Q2} = -i_S D_1 + i_L D_2 \tag{2}$$

$$C_2\frac{dV_2}{dt} = i_{Q3} - i_{Q4} = i_S(1-D_1) - i_L(1-D_2) \tag{3}$$

$$\begin{aligned} &C_1\frac{dV_1}{dt} - C_2\frac{dV_2}{dt} \\ &= -i_S D_1 + i_L D_2 - i_S(1-D_1) + i_L(1-D_2) \\ &= -i_S + i_L \end{aligned} \tag{4}$$

Assuming $C_1 = C_2 = C$, and the voltage unbalance variable ΔV defined as $\Delta V = V_1 - V_2$, then the dynamic equation of ΔV is derived as

$$\Delta V' = \frac{dV_1}{dt} - \frac{dV_2}{dt} = \frac{1}{C}(i_L - i_S) \tag{5}$$

It is clear that the above equation is a first-order linear differential equation. The solution of (5) is given as follows:

$$\Delta V = \frac{1}{C}\int_0^t (i_L - i_S)dt + [V_1(0) - V_2(0)] \tag{6}$$

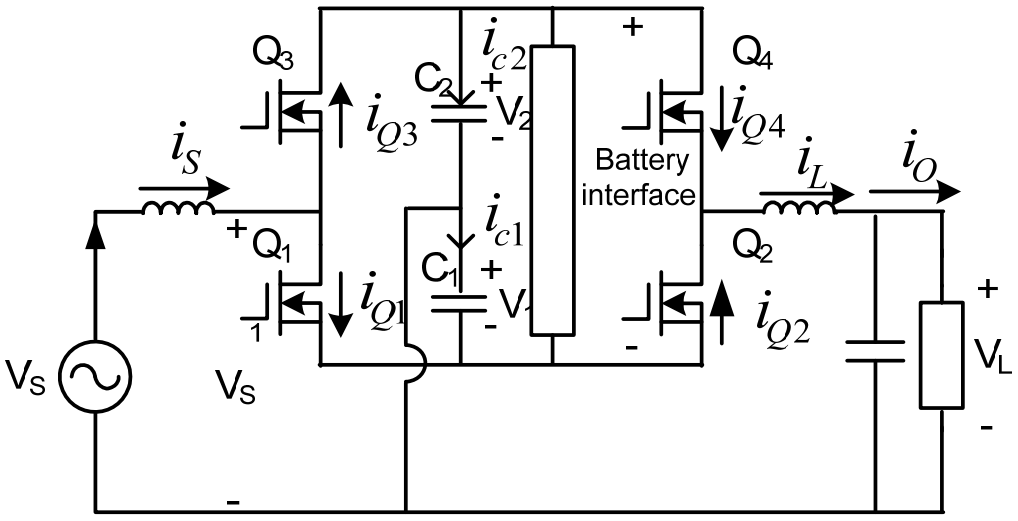


Fig. 1. Single-phase half-bridge AC-AC converter

A. Conventional strategy

In the steady state, i_S follows a sinusoidal command in phase with *Vs*, and i_L is dependent on the load current. Let $i_S = I_S \sin\omega t$, and $i_L = I_L \sin(\omega t + \theta)$, then the following equation can be obtained:

$$\begin{aligned} \Delta V = V_1 - V_2 = &-\frac{I_S}{\omega t}(1-\cos\omega t) + \\ &\frac{I_L}{\omega t}[1-\cos(\omega t+\theta)] + V_1(0) - V_2(0). \end{aligned} \tag{7}$$

It shows that the unbalance caused by the initial conditions of the bus capacitors can not be decayed with time.

To eliminate it, a popular compensation strategy is to sense the unbalance quantity ΔV, and feeding it through a gain block (K_d) into the input current command i_{Sref} [1-2], therefore

$$i_{Sref1} = i_{Sref} + K_d \Delta V. \tag{8}$$

It shows the input current command is replaced by i_{Sref1}. For a closed-loop control system with a well designed inner current controller, the input current will track the current command with the same shape. Thus, the input current response corresponding to the command i_{Sref1} is as follows:

$$i_{S1} = \frac{i_{Sref1}}{K_{ct}} = \frac{i_{Sref} + K_d \Delta V}{K_{ct}} = i_S + K_{d1} \Delta V, \tag{9}$$

where K_{ct} denotes the current loop gain. From (5), $\frac{d\Delta V}{dt}$ is given by

$$\frac{d\Delta V}{dt} = \frac{-i_S - K_{d1}\Delta V + i_L}{C}. \tag{10}$$

Equation (10) is an ordinary first-order differential equation, and can be represented as follows:

$$\frac{d\Delta V}{dt} + \frac{K_{d1}}{C}\Delta V = \frac{i_L - i_S}{C}. \tag{11}$$

Its solution is given by

$$\Delta V(t) = e^{-\frac{K_{d1}}{C}t} \int_0^t e^{\frac{K_{d1}}{C}t'} \left(\frac{i_L - i_S}{C}\right) dt + K e^{-\frac{K_{d1}}{C}t}, \tag{12}$$

where K is obtained from the initial condition of $\Delta V(t)$, by setting time equal to zero. From (12), it is clear that the dc unbalance caused by the initial condition of the dc bus capacitors will approach zero asymptotically in steady state. If i_S and i_L are sinusoidal, then the difference between these two terms will be sinusoidal, and can be given by

$$i_L - i_S = I_d \sin(\omega t + \phi). \tag{13}$$

Thus the steady state solution of $\Delta V(t)$ can be obtained as follows:

$$\Delta V(t) = \frac{\frac{I_d}{\omega C}}{\left(\frac{K_{d1}}{\omega_O}\right)^2 + 1} \left[\cos(\omega t + \phi) - \frac{K_{d1}}{\omega C}\sin(\omega t + \phi)\right]. \tag{14}$$

The above equation shows that even though the dc component of ΔV has been eliminated in steady state, it still has the line frequency components.

However, for the case of dc bias component existing in i_S or i_L, the difference between these two terms will be sinusoidal plus a dc component which can be given by

$$i_L - i_S = I_d(\sin \omega t + \phi) + I_{dc}, \tag{15}$$

where I_{dc} represents the dc component which will contribute a dc bias quantity to ΔV. The contributing quantity can be obtained from (12), and is given as follows:

$$e^{-\frac{K_{d1}}{C}t} \int_0^t e^{\frac{K_{d1}}{C}t'} \cdot \frac{I_{dc}}{C} dt = \frac{I_{dc}}{K_d}(1 - e^{-\frac{K_{d1}}{C}t}). \tag{16}$$

This equation shows that in the steady state, the conventional compensation strategy based on (8) still has a dc

bias which varying linearly with the bias current.

B. The proposed strategy

To eliminate the unbalance in (16), this paper proposed a new compensation strategy which is given by

$$i_{Sref\,2} = i_{Sref} + K_d \Delta V + K_I \int_o^t \Delta V dt', \tag{17}$$

where K_I denotes the scale of the integral. Thus, the input current response corresponding to the command $i_{Sref\,2}$ is as follows:

$$\begin{aligned} i_{S2} &= \frac{i_{Sref\,2}}{K_{ct}} = \frac{i_{Sref} + K_d \Delta V + K_I \int_0^t \Delta V dt'}{K_{ct}} \\ &= i_S + K_{d1} \Delta V + K_{I1} \int_0^t \Delta V dt', \end{aligned} \tag{18}$$

then (11) will be replaced by

$$\begin{aligned} &\frac{d^2 \Delta V}{dt^2} + \frac{K_{d1}}{C} \frac{d\Delta V}{dt} + \frac{K_{I1}}{C} \Delta V \\ &= \frac{1}{C} \frac{d}{dt} (i_L - i_S). \end{aligned} \tag{19}$$

The above equation is a second-order differential equation with constant coefficients. The characteristic polynomial for this differential equation is

$$s^2 + \frac{K_{d1}}{C} s + \frac{K_{I1}}{C} = 0, \tag{20}$$

$$\alpha = \frac{K_{d1}}{2C}, \tag{21}$$

$$\omega_o = \sqrt{\frac{K_{I1}}{C}}, \tag{22}$$

where α is called the damping constant, and ω_o is called the resonant frequency. Note that both α and ω are positive because the related parameters are positive. The zeros of the characteristic polynomial are

$$s_{1,2} = -\frac{K_{d1}}{2C} \pm \sqrt{\frac{K_{d1}^{\,2} - 4K_{I1}^{\,2}}{4C}}. \tag{23}$$

For minimizing the dc bus voltage stress, the overdamped condition is adopted in this paper. Combining (15), (19), (21), (22), the steady state solution of $\Delta V(t)$ can be obtained as follows:

$$\begin{aligned} \Delta V(t) = &\frac{2\alpha \frac{\omega^2}{C} I_d (\sin \omega t + \phi)}{(\omega^2{}_o - \omega^2)^2 + 4\alpha^2 \omega^2} + \\ &\frac{\frac{\omega}{C} (\omega^2{}_o - \omega^2) I_d (\cos \omega t + \phi)}{(\omega^2{}_o - \omega^2)^2 + 4\alpha^2 \omega^2}. \end{aligned} \tag{24}$$

It shows the unbalance caused by the dc bias has been eliminated due to the proposed strategy. For a design

of $\omega \rangle\rangle \omega_0$ and $\alpha \rangle\rangle \omega_0$ the above equation can be simplified as follows:

$$\Delta V(t) \cong \frac{2\alpha \frac{\omega^2}{C} I_d(\sin \omega t + \phi) - \frac{\omega^3}{C} I_d(\cos \omega t + \phi)}{(4\alpha^2 + \omega^2)\omega^2}. \tag{25}$$

III. Control system design

A. Rectifier stage design

Fig. 2 shows the control block diagram of the rectifier stage, where V_{dc}^* is the reference for the sum of V_1 and V_2 . The current command i_s^* is obtained by adding the proposed compensation item derived from $\Delta V(t)$, through a PI block and adding its output into a sinusoidal signal which is in-phase with V_s , then compared with the sensed input current i_s to generate the gate signals for the related switches. $LPF1$ and $BRF1$ are the low pass filter and the band rejection filters, respectively. G_{vi1} is the PI controller for stabilizing the dc bus voltage. G_{PI} is the proposed PI compensator to force the dc value in $\Delta V(t)$ to zero. G_{vdc1} is the low pass filter used to reduce the switching noise.

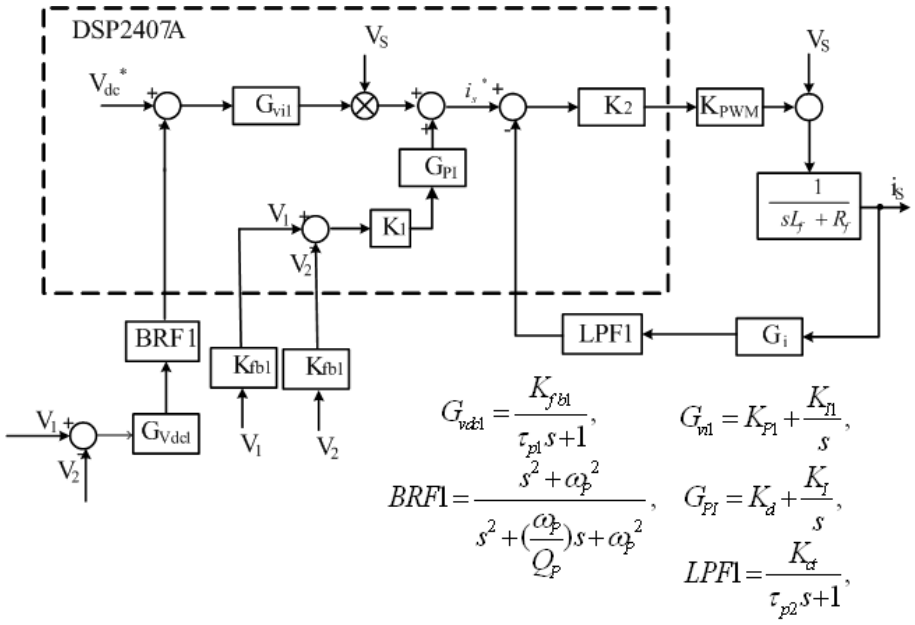


Fig. 2. Control block diagram for the rectifier stage.

B. Inverter stage design

Fig. 3 shows the control block diagram of the inverter stage. It is mainly composed of a dc voltage regulator G_{vi2} for the outer loop, and an ac voltage regulator for the inner voltage loop and current loops. In the outer loop, the average value of the load voltage is detected by the low pass filter G_{bw} circuit and sent to the band rejection filter $BRF2$ which is the same as $BRF1$ for rejecting the 120 Hz ripple component.

C. DC balance design in the inverter stage

As mentioned above, a low-level of DC voltage bias may exist in the inverter output due to the draft of circuit components or half-wave load conditions. To eliminate this condition, a DC balance regulator (DCB) is also necessary for the inverter stage. [7] has pointed out two feasible types of DC balance regulator loops. These two

types of compensation strategies can be used here, and has been included into Fig. 3.

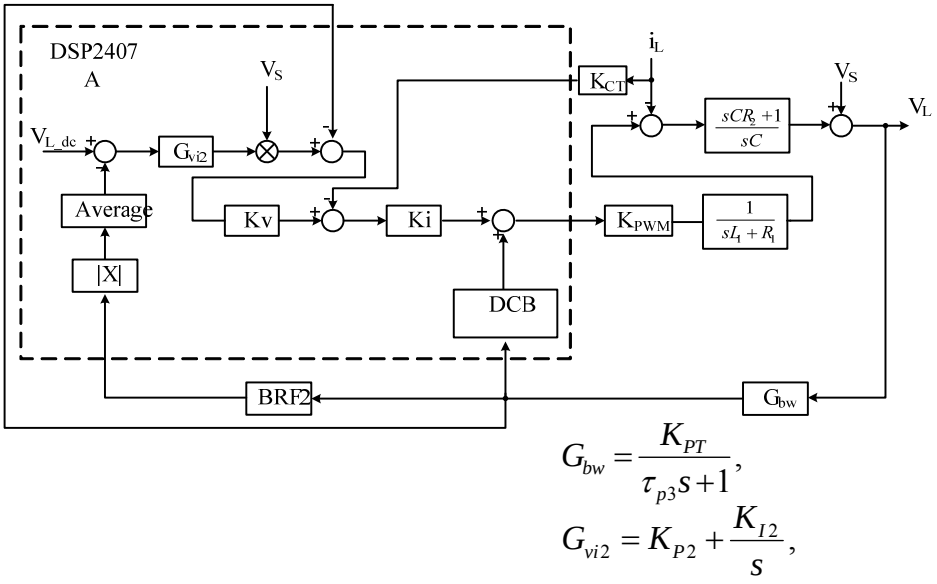
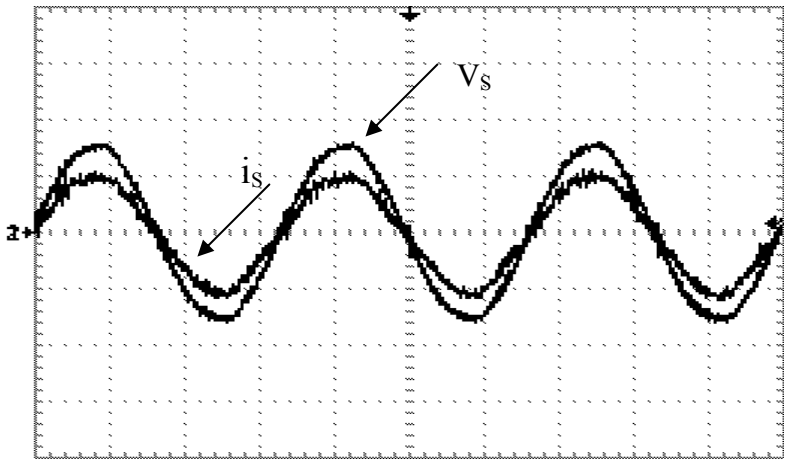


Fig. 3. Control block diagram of the inverter stage.

IV Experimental results

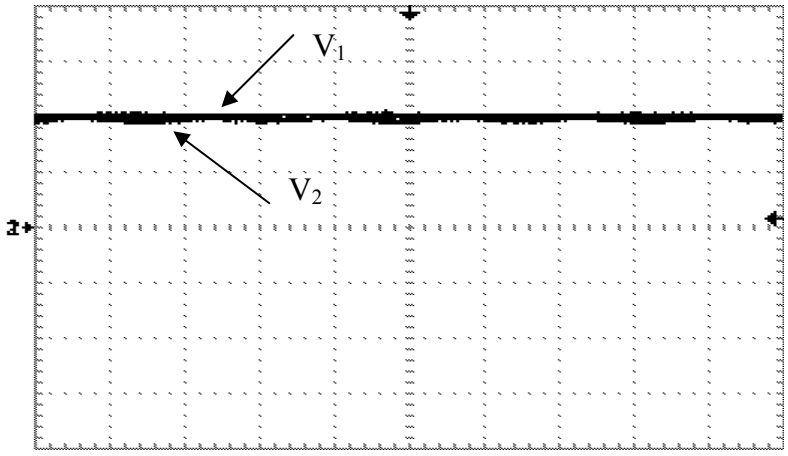
A prototype of 1 kVA system using DSP TMS320LF2407A digital controller has been used to verify the proposed idea. The switching frequency is 18 kHz, and both the two DC bus voltages are regulated at 200 V. The reference sinusoidal signal is generated from a zero-crossing detector.

Figure 4 shows the performance for a balance load case. Fig. 4(a) shows the source voltage and current, Fig. 4(b) shows the two split dc bus voltages, and Fig. 4(c) shows the load voltage and current. It shows the source current has in-phase with the source voltage, and the two split dc bus voltages are balance.



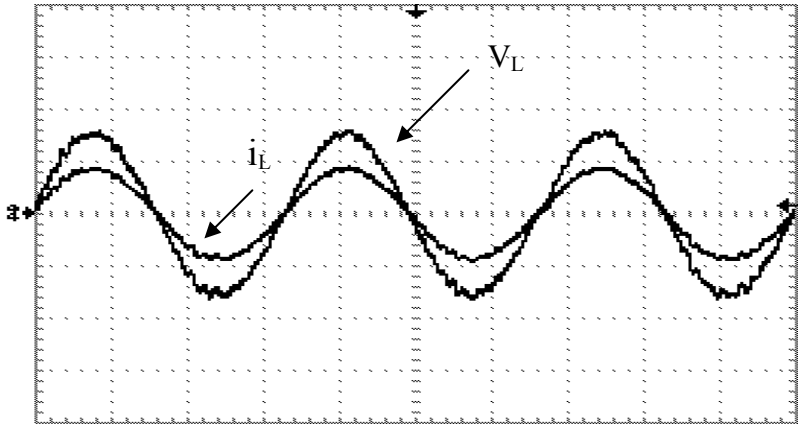
Vs(100V/div) & is(5A/div) 5ms

(a)



V_1(100V/div) & V_2(100V/div)　5ms

(b)

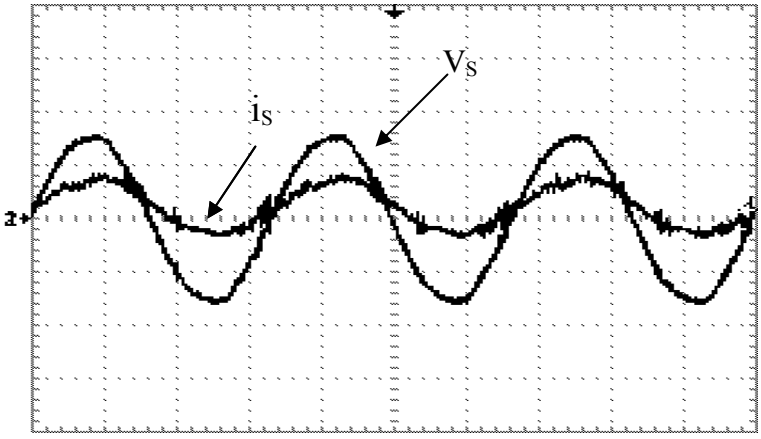


V_L(100V/div) & i_L(5A/div)　5ms

(c)

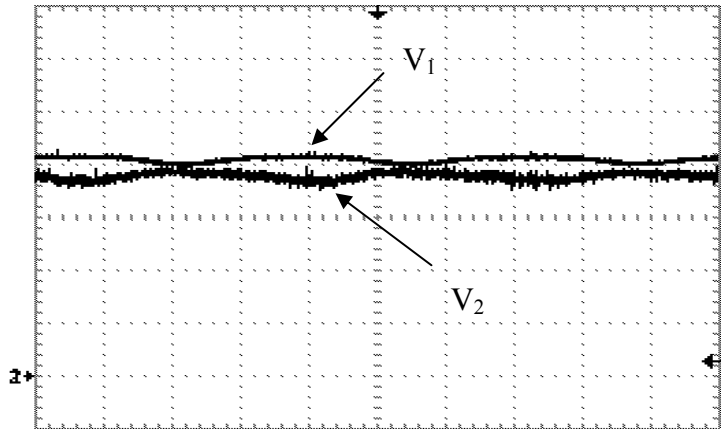
Fig. 4. The experimental results for a balance load case, (a) the source voltage and current, (b) the two split dc bus currents, (c) the load voltages and current.

Figure 5 shows the performance for an unbalanced load, and a traditional P compensation strategy is adopted. It shows that a dc bias above 20V existed, and the larger the unbalance, the larger the dc bias.



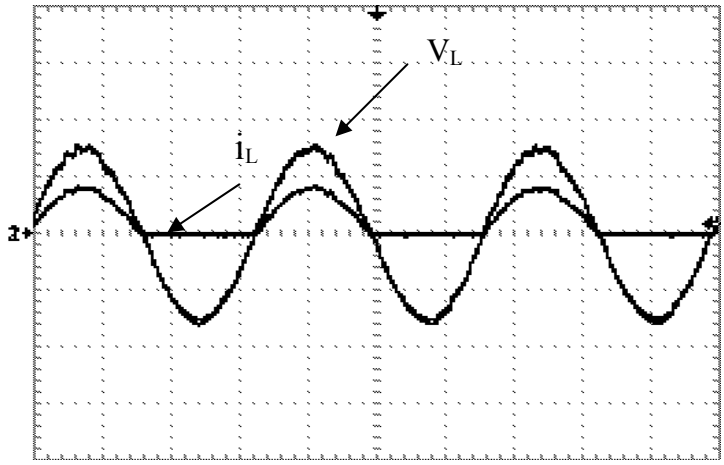
Vs(100V/div) & is(5A/div)　5ms

(a)



V1(50V/div) & V2(50V/div)

(b)

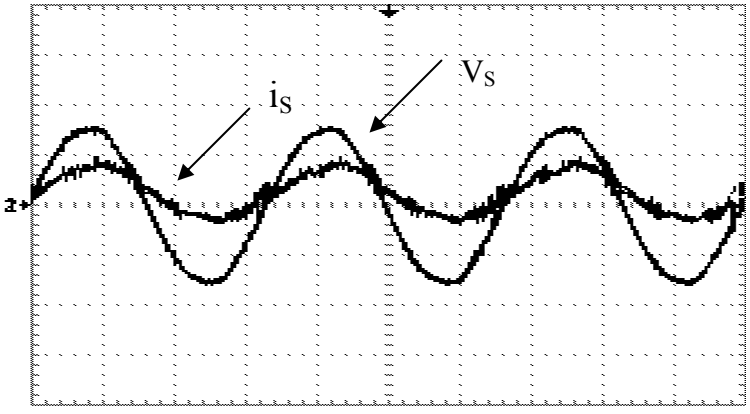


V_L(100V/div) & i_L(5A/div) 5ms

(c)

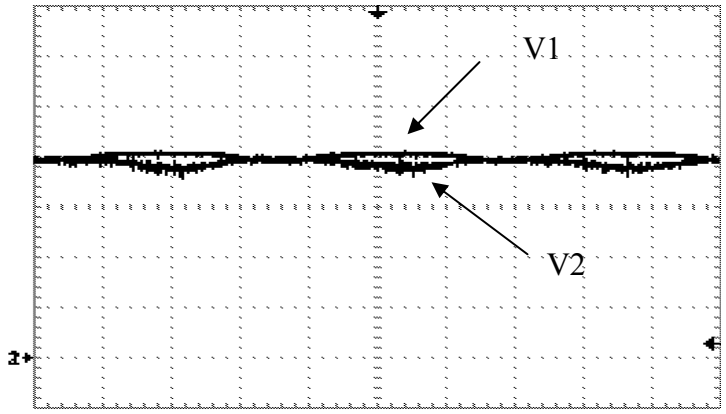
Fig. 5. The experimental results with traditional P controller, (a) the source voltage and current, (b) the two split dc bus currents, (c) the load voltages and current.

Fig. 6 shows the same case with Fig. 5, where the proposed PI compensating strategy is applied (these two cases have the same P parameter). Fig. 6(a) shows the source voltage and current, Fig. 6(b) shows the two split dc bus voltages, and Fig. 6(c) shows the load voltage and current. It shows the dc bias has been reduced.



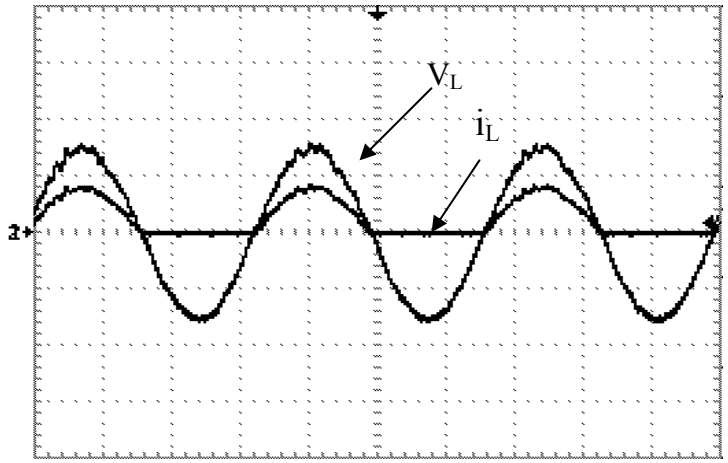
Vs(100V/div) & is(5A/div) 5ms

(a)



V1(50V/div) & V2(50V/div)

(b)

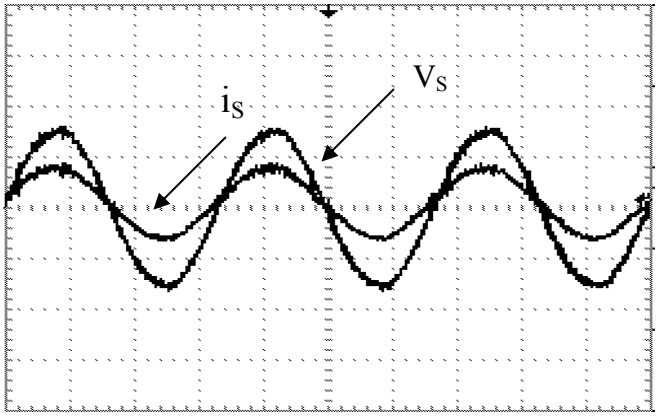


V_L(100V/div) & i_L(5A/div)　5ms

(c)

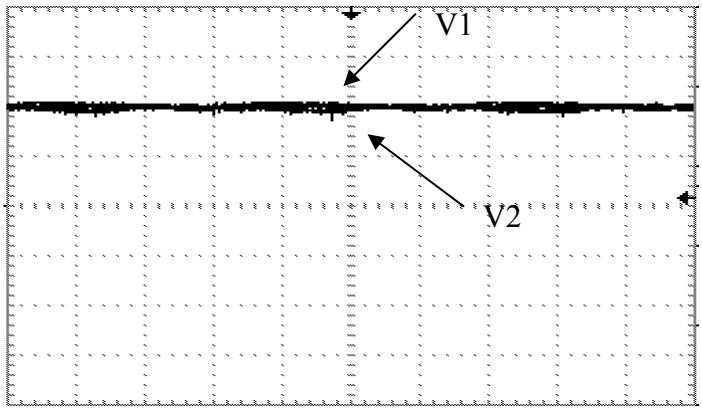
Fig. 6. The experimental results with the proposed PI controller, (a) the source voltage and current, (b) the two split dc bus currents, (c) the load voltages and current.

Fig. 7 shows another case, where the proposed PI compensating strategy is applied. Fig. 6(a) shows the source voltage and current, Fig. 6(b) shows the two split dc bus voltages, and Fig. 6(c) shows the load voltage and current. It shows the dc bias has also been reduced.



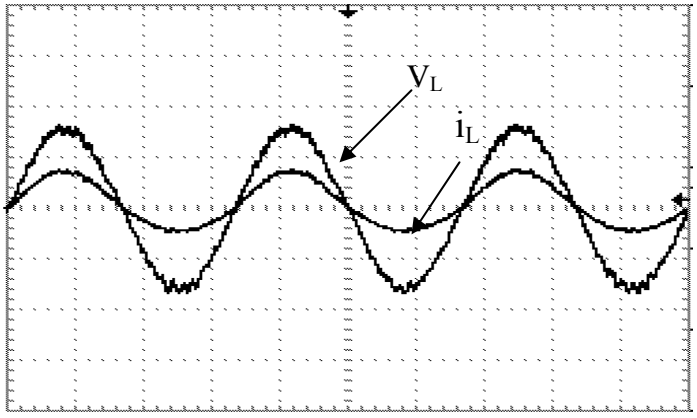
Vs(100V/div) & is(5A/div)　5ms

(a)



V1(50V/div) & V2(50V/div)

(b)

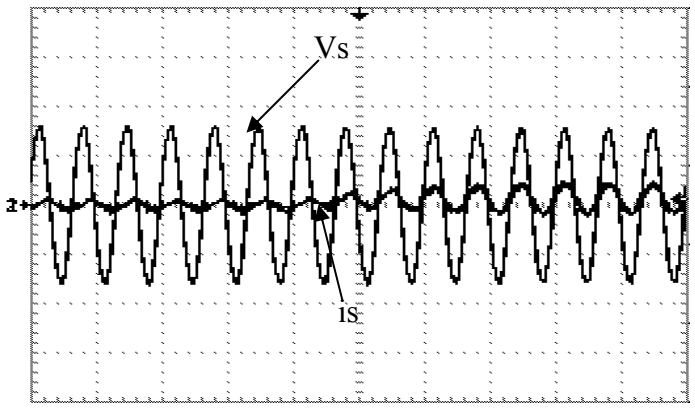


V_L(100V/div) & i_L(5A/div) 5ms

(c)

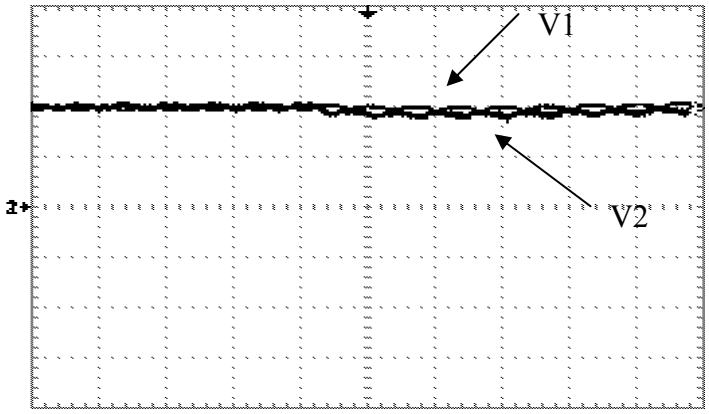
Fig. 7. The experimental results with the proposed PI controller operated in unbalance load case, (a) the source voltage and current, (b) the two split dc bus currents, (c) the load voltages and current.

Fig. 8 shows the transient responses of the proposed PI compensator due to an unbalance load change. Fig. 7(a) shows the source voltage and current, Fig. 7(b) shows the two split dc bus voltages, and Fig. 7(c) shows the load voltage and current. It shows the proposed PI compensator can also maintain the two dc bus voltages against the unbalance load change.



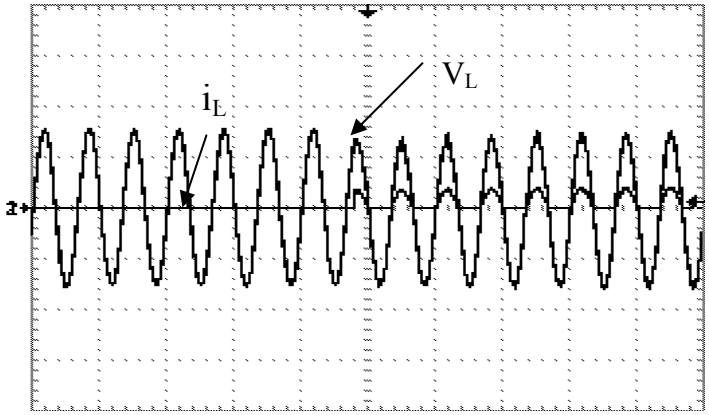
Vs(100V/div) & Is(10A/div) 25ms

(a)



V1(100V/div) & V2(100V/div) 25ms

(b)



V_L100V/div) & I_L10A/div) 25ms

(c)

Fig. 8. The transient response for an unbalanced load change, (a) the source voltage and current, (b) the two split dc bus voltages, (c) the load voltage and current.

V Conclusions

A single-phase half-bridge AC-AC converter has been described. A novel and effective control strategy which provides the benefits of eliminating the dc bias existed in dc bus voltages has been confirmed. It is able to achieve low cost and high efficiency due to a reduced number of semiconductors. It is easy to implement by DSP based digital controller. Prototype results have shown the proposed system to be suitable for any load type of voltage variation, especially in the case of half-wave loads, and therefore a very valuable innovation.

VI. Acknowledgments

This work has been supported by National Science Council, Republic of China under research project NSC94-2622-E-218-018-CC3.

VII. References

1. R. Srinivasan, R. Organti, “A unity power factor converter using half-bridge boost topology,” IEEE Trans. on Power Electronics, 1998, 13, (3), pp. 487-500.

2. C. T. Ho, J. M. Wang, Y. K. Lo, " Analysis and elimination of the output voltage unbalance for a half-bridge boost rectifier under mismatched loads, "IEEE PESC'06 Conf,. 2006, pp. 1-3.
3. G. Narayanan, R. Ghosh, "A simple analog controller for single-phase half-bridge rectifier," IEEE Trans. on Power Electronics, 22, (1), 2007, 186-198.
4. Chen, C.C., and Divan, D.M., "Simple topologies for single phase as line conditioning," IEEE Trans. Ind. Appl., 1994, 30, (2), pp. 406–412.
5. Cheng, Y.C., Chen, D.K.W., and Lee, Y.S., "Design of a novel ac regulator," IEEE Trans. Ind. Electron., 1991, 38, (2), pp. 89–94.
6. C. B. Jacobina, E. R. C. da Silva, T. M. Oliveira, "Control of the single-phase three-leg AC/AC converter," IEEE Trans. Ind. Electron., 2006, 53, (2), pp. 467–476.
7. M. T. Tsai, "Analysis and design of a cost-effective series connected AC voltage regulator," IEE Proc-Electr. Power Appl., 151, (1), 2004, pp. 107-115.