The design of a Sigma-Delta Modulator for multi-standard communication system applications

Hwi-Ming Wang[1], Chi-Yuan Huang[2]
Department of Electrical Engineering of Southern Taiwan University, Tainan, Taiwan[1,2]
tonywang@mail.stut.edu.tw[1], m9620210@webmail.stut.edu.tw[2]

Abstract

This paper proposes a multi-bit sigma-delta modulator (SDM) for dual-mode communication applications. The SDM can be applied to GSM/WCDMA systems. The structure for the designed SDM is chosen as a single-stage, third-order, 3-bit feedforward(FF) structure to meet the design target specifications. The SDM is operated at sampling frequencies of 13MHz/46.08MHz for GSM/ WCDMA modes, respectively (equivalently oversampling ratio of 65 and 12). The SDM is designed in TSMC 0.18μm 1P6M CMOS technology. At 3.3V power supply, simulation results show that, the proposed SDM can achieve the signal to noise plus distortion ratio (SNDR) of 87.52dB/70.03dB and total power consumption of 12.2mW/15.4mW for GSM/WCDMA, respectively.

Introduction

Under the dual-mode operation, the analog-to-digital convertors (ADC) in the receiver chain have to contain kinds of demand of bandwidth and resolution. The ADC must provide the different specification for different communication system. SDM can be the best choice, because it can achieve this demand by the method of programmable characteristic. The purpose of programmable design is based on the specification of communication system and dynamic range (DR) to choose SDM architecture (include: number of order, OSR and number of bit of quantizer) to meet the specification of the communication system needed. Fig.1 shows the SDM system block diagram proposed for this paper.

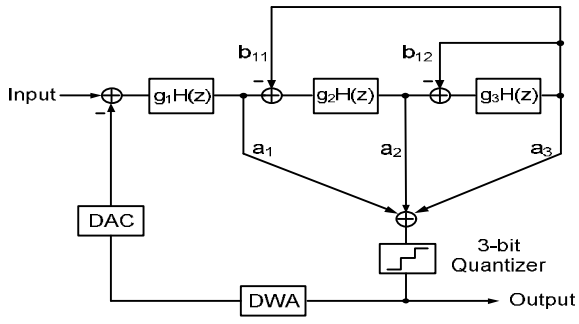

Fig.1 The system block diagram of SDM

Experimental Results

This paper combines the use of HSPICE and MATLAB to simulate and calculate its performance. Fig.2 and Fig.3 shows the modulator output spectrum for GSM/WCDMA mode with the input amplitude of -6dB. Fig.4 presents the DR for GSM/WCDMA mode. It shows a peak SNDR of 90dB@-5dB in GSM mode and peak SNDR of 72dB@-3dB in WCDMA mode.

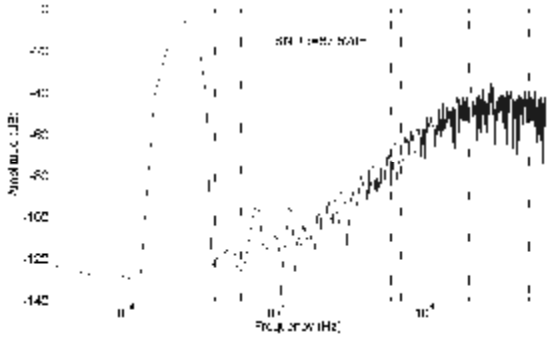

Fig.2 Modulator Output Spectrum for GSM mode

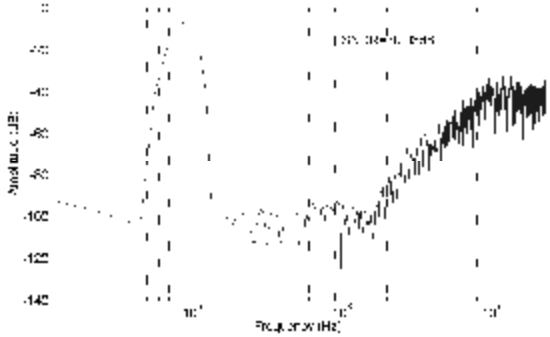

Fig.3 Modulator Output Spectrum for WCDMA mode

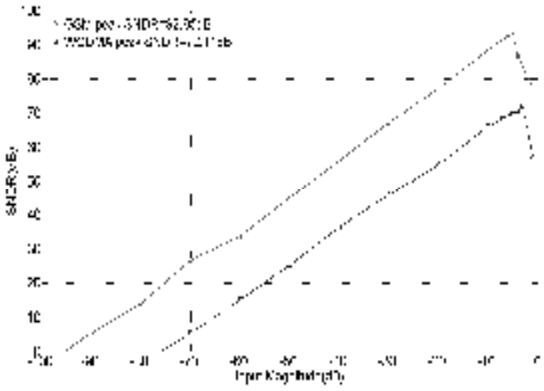

Fig.4 Dynamic Range plot for GSM/WCDMA mode

Conclusion

This paper proposes a dual-mode SDM design for GSM/WCDMA applications. It employs a single-stage, third-order, 3-bit feedforward SDM to meet GSM/WCDMA specifications. The SDM is designed in TSMC 0.18μm 1P6M CMOS technology, which operated at sampling frequencies of 13MHz/46.08MHz and OSR of 65/12 for GSM/WCDMA modes, respectively. The simulation results show that, the proposed SDM can achieve SNDR of 87.52dB/70.03dB and power consumption of 12.2mW/15.4mW, respectively.