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A NOVEL PARALLEL-COUPLED LINE DIPLEXER EXCITED USING SLOT-LINE RESONATORS FOR ULTRA-WIDEBAND COMMUNICATIONS

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ABSTRACT: *In this letter, a novel design of microstrip diplexer used for ultra-wideband communication has been proposed. The primary structure of the diplexer comprises two different parallel-coupled line structures with slot-line resonators (SLRs), which are used for generating the filtering response with high-channel selectivity. The diplexer is designed to have the lower and higher passband with the operating frequencies at 3.2–4.8 GHz and 6.5–9.8 GHz, respectively. Experimental results also show a good agreement with the simulated results.* © 2009 Wiley Periodicals, Inc. Microwave Opt Technol Lett 51: 1552–1555, 2009; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.24356

Key words: *parallel-coupled line; diplexer; ultra-wideband (UWB); bandpass filter (BPF); slot-line resonator (SLR)*

1. INTRODUCTION

Since February 2002, U.S. Federal Communications Commission (FCC) authorized the unlicensed use of Ultra-Wideband (UWB, 3.1–10.6 GHz) for a variety of applications. Design of key components such as antennas or filters used for UWB systems have attracted much attention. The UWB filters are required to have a specified passband with a 110% FBW (defined as 3 dB bandwidth over the center frequency) at the central frequency of 6.85 GHz. However, to avoid the interference from the frequency use of 5–6 GHz for IEEE 802.11a wireless local area networks (WLANs), the direct sequence ultra-wideband (DS-UWB) specifications for wireless personal area networks (WPANs) need further to divide into two regions of 3.1–4.9 GHz and 6.2–9.7 GHz [1].

In general, diplexers are three terminal devices which let two or more frequencies into one input port and then separate them to two other output ports. In the past, several methods have been reported to develop diplexers as follows [2-5]. In Ref. 2, two periodic filter structures with open-circuited stubs were used. In Ref. 3, the stepped impedance coupled-line resonators were used to realize the high isolation hairpin line diplexer. In Ref. 4, a diplexer was formed by combining of two filters, which are constructed with some common resonators sections. In Ref. 5, a novel microstrip diplexer structure composed of a dual-passband filter together with two matching circuits was proposed. However, the aforementioned diplexers in fact have some problematic issues between them, such as large size or high insertion loss. Additionally, there are few papers concerning UWB application. In a previous work, a UWB diplexer was designed by using two hairpin line filtering structures. The authors use the tapped open stub to introduce an attenuation pole to suppress the spurious response and therefore achieve the high isolation [6].

In this letter, a novel compact microstrip diplexer is proposed for satisfying the future DS-UWB application. Two kinds of microstrip parallel-coupled line structures are used to implement

compact bandpass filters to achieve the required passbands for lower band and higher band of UWB system. After optimizing the performances using full-wave electromagnetic (EM) simulator [7], the proposed diplexer is implemented to experimentally verify the proposed design method.

2. DIPLEXER STRUCTURE AND DESIGN PROCEDURE

In our design, the diplexer uses two parallel-coupled line filters with open- and short-circuited at one end. The required passbands of the two different parallel-coupled line filters are excited by using the slot-line resonators (SLRs) [8]. The simulated responses of the parallel-coupled lines with the terminal loads (Z_L) used in the filter design are shown in Figure 1. First, the characteristics of the transmission zeros for the parallel-coupled lines are derived from the classical analysis of even- and odd-mode excitation. The even- and odd-mode input impedances Z_{ine} and Z_{ino} of the parallel-coupled line filters are given as follows [9]:

$$Z_{ine} = Z_{0e}\frac{Z_L + jZ_{0e}\tan\theta_e}{Z_{0e} + jZ_L\tan\theta_e} \quad (1)$$

$$Z_{ino} = Z_{0o}\frac{Z_L + jZ_{0o}\tan\theta_e}{Z_{0o} + jZ_L\tan\theta_o} \quad (2)$$

where Z_{0e} and Z_{0o} are the characteristic impedances of the coupled lines, θ_e and θ_o are the electrical lengths for even- and odd-mode excitations, respectively. It is known that the condition for the transmission zero, namely $S_{21} = 0$, is $Z_{ine} = Z_{ino}$ [9]. The condition for obtaining the transmission zeros location of parallel-coupled line as $Z_L = 0$ for short-circuited and $Z_L = \infty$ for open-circuited can be derived as following equations, respectively:

$$Z_{0o}\cot\theta_o = Z_{0e}\cot\theta_e \quad (3)$$

$$Z_{0e}\cot\theta_o = Z_{0o}\cot\theta_e \quad (4)$$

For obtaining the good stopband performance of the proposed filter, the electrical length of the microstrip parallel-coupled lines with open-circuited and short-circuited are equivalent to quarter-wavelength at central frequency 4 GHz and half-wavelength at central frequency 8 GHz, respectively. In this work, for the two designed parallel-coupled lines filters, the physical lengths are all 14.3 mm and the Z_{0e} and Z_{0o} of the coupled lines are 159.73 Ω and

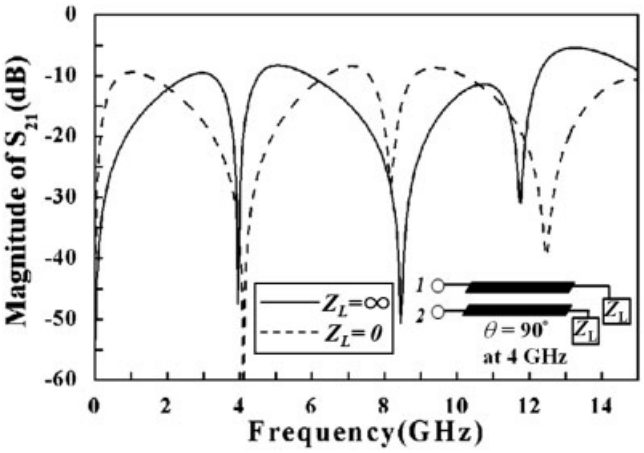

Figure 1 Simulated frequency responses of the parallel-coupled lines with open and short at one end

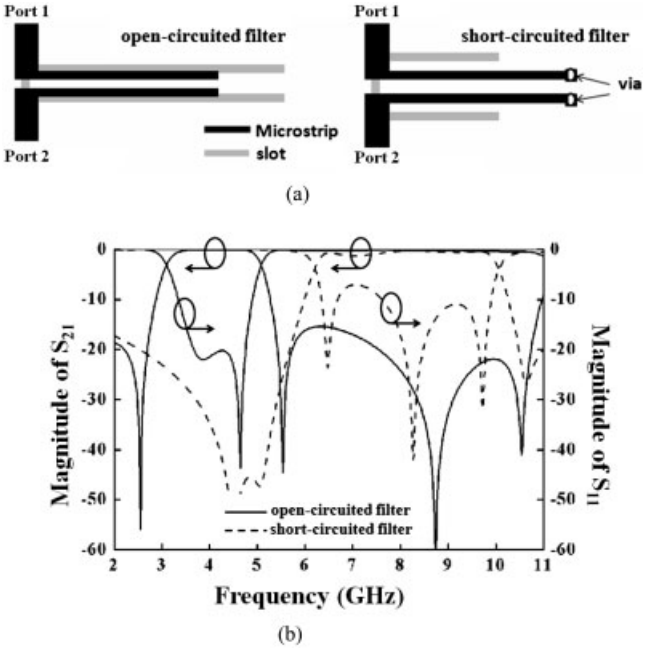

Figure 2 (a) Layouts and (b) simulated responses of the open- and short-circuited bandpass filters

90.01 Ω, respectively. It is clearly observed that the structures can exhibit all-stop response with multiple transmission zeros, which appear at 4, 8, and 12 GHz for both circuits.

To excite the wide passband response, the slot-line resonators (SLR) under the parallel-coupled lines are used, as discussed in the previous work [8, 10]. Figure 2(a) shows the layouts and Figure 2(b) shows the individual simulated results of the two designed filters. Two wideband filters were designed for the center frequency of 4 and 8 GHz, respectively. The filter centered at 4 GHz is denoted as the open-circuited filter and the filter with center frequency of 8 GHz is denoted as the short-circuited filter. It is clearly observed that the isolation between the two passbands is 28 dB at 5.6 GHz.

Figure 3(a) depicts the layout of the proposed microstrip diplexer by combining the two individual filters. The common input port is Port 1, and the output port for lower band and higher band is Port 2 and Port 3, respectively. To obtain the high isolation between the two filters, the stub lengths L_4, L_5, and L_6 of the Port 1 should be well-designed to satisfy the following conditions. When the short-circuited filter is operated, the input impedance seen into the open-circuited filter is infinite and when the open-circuited filter is operated, the input impedance seen into the short-circuited filter is infinite [2–6]. The optimum stub lengths L_4, L_5, and L_6 of the Port 1 are obtained by the full-wave EM analysis. The simulated response of the diplexer is shown in Figure 3(b). The simulated responses show that the lower passband is designed with the passband range of 3.1–4.9 GHz and the higher passband is designed with the passband range of 6.5–9.8 GHz. In addition, the wide stopband rejections of the two functional channels are achieved since the multitransmission zeros are introduced by the parallel coupled-line resonators.

In our design, the proposed filter is implemented on the RT/Duroid 5880 with a dielectric constant of $\varepsilon_r = 2.2$, a loss tangent of 0.0009, and a thickness h of 0.787 mm. The circuit parameters of the proposed microstrip diplexer are $L_1 = 14.3$ mm, $L_2 = 14.3$ mm, $L_3 = 7$ mm, $L_4 = 7.4$ mm, $L_5 = 11.4$ mm, $L_6 = 5.2$ mm, $L_7 = 3.9$ mm, $L_8 = 6.3$ mm, $W_1 = 2.4$ mm, $W_2 = 0.4$ mm, $W_3 = 0.4$

mm, and G_1 = 0.4 mm, G_2 = 0.8 mm, G_3 = 1.6 mm. The input/output ports are all designed for 50 Ω. Simulation and optimization were done using IE3D simulator.

3. EXPERIMENTAL RESULTS AND DISCUSSION

The proposed diplexer is then fabricated and measured by an HP8510C Network Analyzer. The photographs of the fabricated filter, including the front and bottom views, are showed in Figure 4 (a). The comparison between the simulated and measured results is displayed in Figure 4 (b). The isolation between the two passbands is better than 15 dB. The DS-UWB diplexer at lower passband has good measured results, including a center frequency f_0 of 4 GHz, low S_{21} of -1.4 ± 0.3 dB, a wide bandwidth of 3.1–4.8 GHz (FBW 42%), and a wide stopband rejection greater than 20 dB from 6.8 to 11 GHz. The DS-UWB diplexer at higher passband also shows good measured results, including a center frequency f_0 of 8.2 GHz, low S_{21} of -2.4 ± 0.5 dB, a wide bandwidth of 6.4–10.2 GHz (FBW = 42%), and a wide stopband rejection greater than 18 dB from 1 to 5.9 GHz. In addition, the fabricated diplexer occupies a small size, around 23 mm × 20 mm. In addition, the proposed microstrip diplexer is realized on low-cost commercial substrate without using expensive lithography process. Therefore, it has a good potential for the DS-UWB communication due to its very simple design, compact size, and easy fabrication. Measured results are slightly different from the simulated results. The mismatch could be attributed to a misalignment between the top and bottom patterned circuits during the fabrication [11].

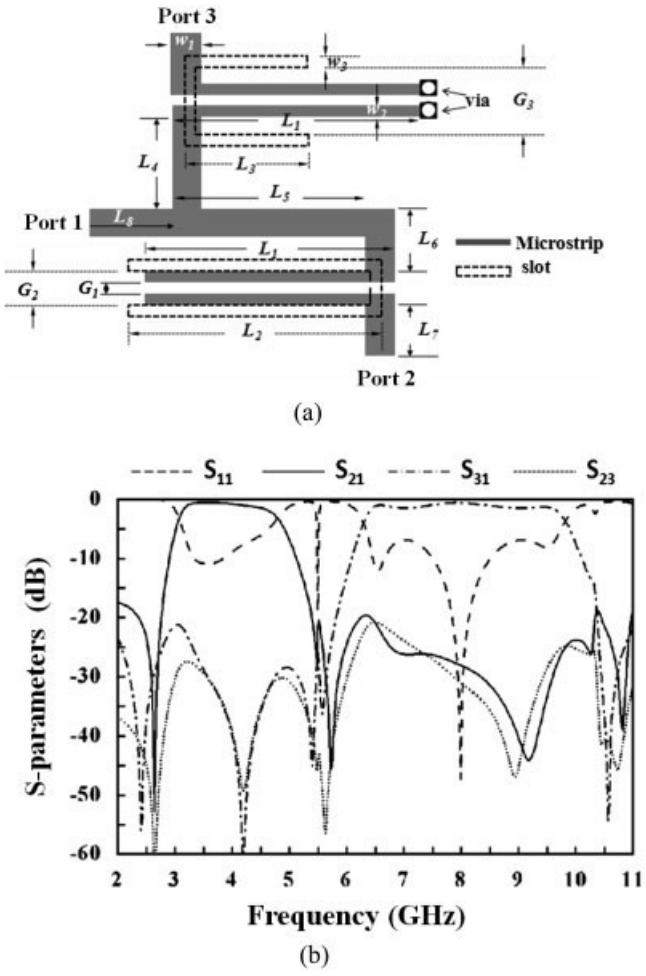

Figure 3 (a) Layout and (b) simulated response of the diplexer

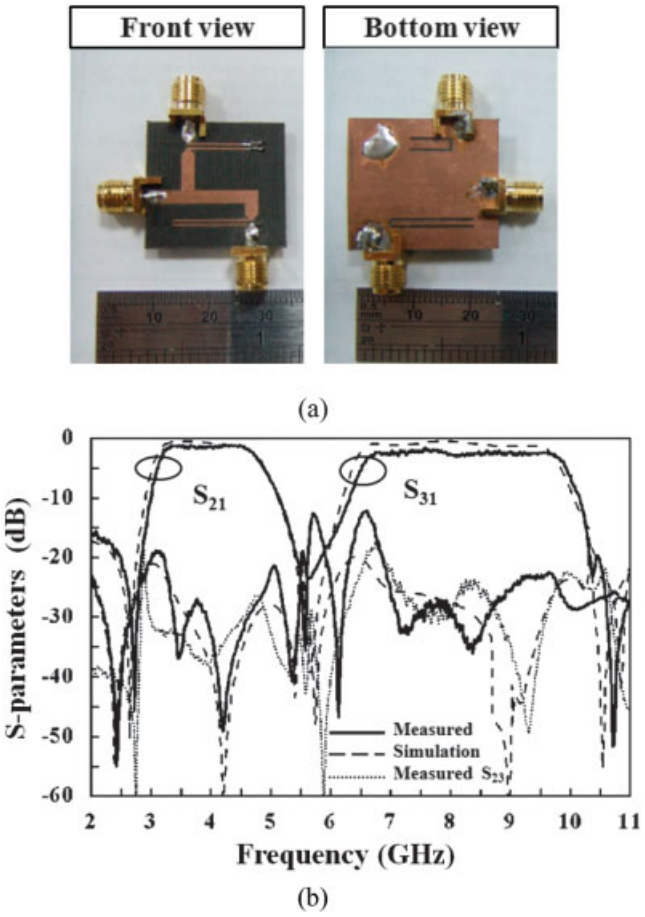

Figure 4 (a) Photography and (b) simulated and measured frequency response of the fabricated diplexer. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

4. CONCLUSIONS

In this letter, design of a novel compact microstrip diplexer has been proposed to satisfy the future DS-UWB application. The characteristics of two kinds of parallel-coupled line structures are thoroughly investigated to make the best use of them in bandpass filters and diplexer designs. The design procedure is based on the classical analysis of even- and odd-mode excitation. The proposed microstrip diplexer has two passbands operated at 3.1–4.8 GHz and 6.4–10.2 GHz corresponding to the considered specification. The measured results of the fabricated diplexer actually verify the proposed design concept and match with the simulated results.

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A SIX-PHASE DIVIDE-BY-3 INJECTION LOCKED FREQUENCY DIVIDER IN SiGe BiCMOS TECHNOLOGY

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ABSTRACT: *This article presents a six-phase silicon-germanium (SiGe) heterojunction bipolar transistor divide-by-3 injection locked frequency divider (ILFD). The ILFD is based on a three-stage differential ring oscillator (voltage controlled oscillators) and was fabricated in the 0.35 μm SiGe 3P3M BiCMOS technology. The divide-by-3 function is performed by injecting a differential signal to the common gates of injection MOSFETs with the drain/sources connected to the VCO outputs. Measurement results show that when the supply voltage* V_{dd} *is tuned from 1.4 V to 2 V, the divider free-running oscillation frequency is tunable from 6.2 GHz to 3.58 GHz, and at the incident power of 0 dBm the operation locking range is about 8.3 GHz, from the incident frequency 18.8 to 10.5 GHz. The core power consumption is 8.96 mW at* V_{dd} *= 1.4 V. The die area is 0.802 × 0.812 mm*^{2}. © 2009 Wiley Periodicals, Inc. Microwave Opt Technol Lett 51: 1555–1557, 2009; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.24345

Key words: *SiGe HBT BiCMOS; six-phase; divide-by-3 injection-locked frequency divider; locking range; ring-oscillator*

1. INTRODUCTION

Voltage controlled oscillators (VCOs) and frequency dividers (FDs) are two crucial circuits in radio-frequency systems. In applications such as clock-and-data recovery and RF down conversion, several clock phases are required. Recently, multiphase oscillators [1–6] been used in RF systems to improve the performance of system. This article proposes a six-phase injection-locked divider circuit (ILFD), which is a divide-by-3 FD and was implemented with the SiGe heterojunction bipolar transistor (HBT) BiCMOS technology.

Traditionally, multiple clock phases are generated by rings of delay stages. Alternatively, a master VCO and a slave multiphase FD can be combined to provide multiphase outputs. The latter approach is attractive because the ILFD tracks the phase of master VCO and provides accurate phase spacing. The design procedure consists of the design of a low phase noise VCO and the design of a low-power FD with small phase error. There have been existence of divide-by-3 CMOS FDs implemented with either differential LC tank oscillator [7, 8] or three-phase ring oscillator [9]. None of these are implemented with SiGe BiCMOS technology. In conjunction with a master VCO, the proposed six-phase ILFD can be used in a down-conversion receiver [1].

2. CIRCUIT DESIGN

The proposed six-phase divide-by-3 SiGe BiCMOS frequency divider shown in Figure 1 is based on a ring oscillator, which consists of three differential amplifiers by connecting the outputs of each amplifier to the inputs of other amplifier in a feedback loop, thus forming a ring structure. The oscillator provides six outputs with 60° phase shift. The resistors R1 and R2, HBTs Q1 and Q2, tail MOSFET M1 form a differential amplifier. Two pairs of three MOSFETs are used as injectors to coupling external injection signals to the ring oscillator to force the core oscillator to track its phase and frequency with the injection source within the locking range. The injection MOSFETs M_{ji} (i = 1–6) are biased at the injection bias V_{inj} and the differential injection signals are applied to the common gate nodes of injection MOSFETs. In time domain, the oscillation frequency of a ring oscillator is determined by the delay time associated with the charging and discharging of parasitic capacitors. Thus, the fundamental oscillation frequency is given by $f_{osc} = 1/6\tau_d$, where τ_d is the delay through each stage and it is determined by R_O the output resistance and C_L the capacitance at the inverter output node. The capacitance C_L is dominantly controlled by C_{be} the base-emitter junction capacitance of HBT. The capacitance C_{be} comes from both the emitter-base junction

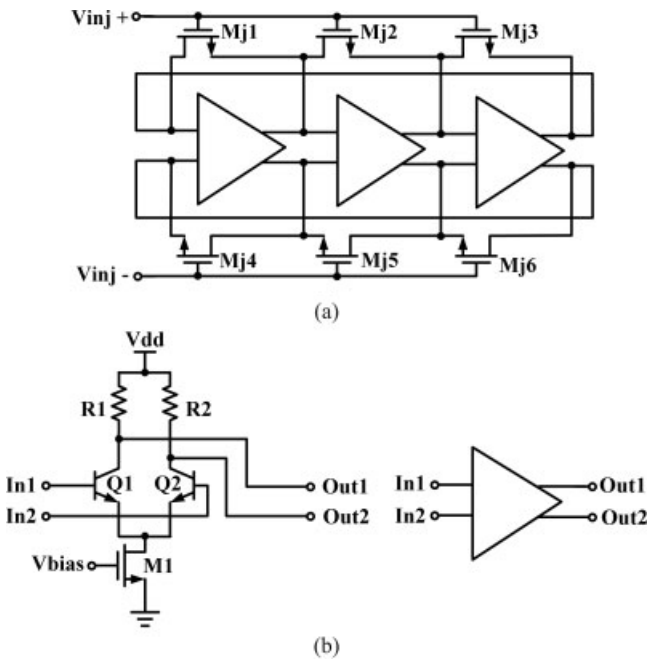

Figure 1 (a) Schematic of the proposed SiGe HBT 6-phase divide-by-3 ILFD. (b) Implementation of one-stage differential amplifier