A Compact Topology for Single-Phase Line-Interactive UPS Using Small DC-Link Capacitor

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Abstract

A novel pulse-width modulated (PWM) single-phase line-interactive uninterruptible power supply (UPS) based on the small dc bus capacitor is presented. The proposed system is made up of an ac chopper which includes a diode rectifier, a boost switch, a charger and an inverter. It has the features of a small dc bus capacitor, small input and output inductors, and low switching loss, and is very suitable for those loads which are with high power factor. It can regulate the sustained voltage swells and sags by controlling the corresponding power switches in the normal mode, and can be switched to back-up mode when the utility voltage fails. Regardless of voltage swells or sags, there is only one power stage switching in PWM status, therefore the proposed topology gives high efficiency. Theoretical analysis has been achieved with detailed analysis. Case study is demonstrated by means of a DSP based prototype experiment to prove its performance and effectiveness.

Index Terms—Line-interactive, AC chopper, Charger.

I. Introduction

Uninterruptible power supplies (UPSs) have been used in many applications, such as medical facilities, computer and data storage systems, telecommunication and industrial processing systems, and so on…, to provide the sensitive loads with uninterrupted and high quality power. They need to protect these critical loads against utility outages as well as voltage swells and sags. UPSs are classified into three topologies [1]–[4]: off-line UPS, line-interactive UPS, and online UPS. These terms refer to UPS operation with respect to utility power. For the off-line UPS, the load is supplied with the utility line in normal mode, and the battery charging. When the utility voltage goes outside the specified tolerances or fails, the battery ensures continuous supply of power to the load with a very short switching time (generally less than 10 ms). The off-line UPS system may have the capability of voltage regulation, however, additional devices, such as a tap changing transformer, must be incorporated into the system to provide the function. The line-interactive UPS has the ability to include limited voltage regulation and an active power filter function, but the load frequency is dependent on the utility line. It is less costly than the on-line UPS. The on-line UPS continuously supplies the load via the rectifier/charger and the inverter (ac/dc/ac) in both normal and abnormal utility conditions. As the energy goes through double-conversion, the load voltage, load frequency and the utility current can be controlled independently. When the utility line fails, the inverter and battery continue to support load power. Thus, this type of UPS system provides continuous protection against utility voltage changes. The on-line UPS is widely recognized as the superior topology in performance, especially for the very wide tolerance to the source voltage variation and very precise regulation of the load voltage. However, they need two power stages, as a consequence, suffer from a big number of power switches, and high switching loss, resulting in this topology is usually the most costly and low efficiency.

Generally, the cost reduction is achieved by reducing the number of power switches or by developing new topologies that employ switches with lower voltage stresses [5-7]. For a single-phase system, the half-bridge rectifier-inverter topology which requires a relatively little number of power switches can fulfill the requirement of cost reduction [8]. However, it is worth to highlight the dc bus voltage unbalance problem in accordance with this topology. The unbalance voltages may be resulted by the small dc variation in the circuit components and controllers, or the load characteristic. A small dc offset in the controller's analogue components could make a possible variation, resulting in the dc bus voltage to become unbalance with respect to the neutral point, while still maintaining a total bus voltage to equal to the reference. This means that it needs a more complicated control algorithm. In addition, there is no help in reducing the switching loss and voltage stress.

In this paper, an improved single-phase line-interactive UPS is proposed for low cost applications. The proposed system is made up of an ac chopper [9-10], and is composed of an diode rectifier, a boost switch, a dc/dc charger and a full-bridge inverter. It has a compact power circuit configuration with the features including a small dc bus capacitor and small input/output inductors, a very simple control algorithm, an enhanced voltage regulation capability, low voltage stresses in power switches, and a low switching loss which indicates a high efficiency. The proposed system can work well in high power

factor loads, such as resistive load and rectifier load. With the proposed control algorithm, it can regulate the sustained voltage swells and sags by controlling the corresponding power switches in the normal mode, and can be switched to back-up mode when the utility voltage fails. Theoretical analysis has been achieved with detailed analysis. Operations, features, and characteristics are verified by the experimental results from a 1-kVA TMS320LF2407AP DSP based prototype.

II. System description

Fig. 1 shows the circuit diagrams of the proposed single-phase UPS. It includes one-diode type, and two-diode type which are shown in Fig. 1(a) and Fig. 1(b), respectively. Fig. 1(a) is similar to a typical PFC scheme except that the small dc bus capacitor. This structure has been popularly used in conventional rectifier with PFC function as it is simple and low cost. However, it has the disadvantage of high conduction loss since there are always three power semiconductors in the current flow path. Fig. 1(b) uses two diodes to reduce the conduction loss since it always has two diodes in the current flow path. Even though the proposed system is similar to the conventional ac/dc/ac topology, the controller is quite different. In this paper, AC chopping technique is adopted instead of the conventional two-stage PWM method. Based on the presented idea, the inductances of the input/output inductors have been substituted by small ones. In addition, the small capacitor to replace the big electric capacitor which used in the conventional structure implies that the proposed system exhibits a compact structure.

The proposed system consists of following blocks:

1) Boost rectifier: It includes both a full-bridge diode and a boost switch. The boost switch is not for correct the input power factor, but for boost the source voltage to the desired level. The input power factor is determined by the load characteristic. This stage may work in continuous or discontinuous conduction mode according to the load characteristic.
2) Inverter stage: It is built of a full bridge topology, and is with 60 Hz switching or PWM switching to regulate the load voltage in accordance with the source voltage variation.

A. Normal Mode operation

In normal source voltage circumstance, the proposed system is cascaded between the source and load, and acts to compensate for utility voltage fluctuations by maintaining a sinusoidal load voltage with a constant root mean square (RMS) value whose phase is very close to the utility voltage. It is intrinsically the on-line UPS structure, and is with huge voltage regulation ability. However, it is still the line-interactive scheme since the load frequency can be changed in this structure.

When the voltage swell occurred, the boost switch is operated in PWM pattern to regulate the load voltage, while the full bridge inverter is switched at 60 Hz [11]. Fig. 2(a) shows the corresponding waveforms in this case. When the voltage sag occurred, the boost switch will be off, and the full bridge inverter is switched at high frequency to maintain the load voltage. Fig. 2(b) shows the corresponding waveforms in this case. Based on the above statements, it is clear that there is only one power stage to be switched in high frequency status whenever the system works. This feature is important

to reduce the switching loss since the proposed structure is consisted of two power stages. As the proposed dc bus voltage is pulsation, it is easy to obtain a sinusoidal output simply by using a dc-level control signal to compare with a triangular waveform. This means the control algorithm here will be less complicated than the conventional method.

B. Backup mode operation

When the utility source fails, the relay connector will be changed-over to the backup mode. In this mode, the load power is supplied by the battery bank, and the boost switch will be operated at high frequency PWM to regulate the load voltage. As the boost structure can not be used to step-down the output to be lower than the input, a 60Hz switching strategy here will distort the output waveform. Fig. 2(c) shows the corresponding switching pattern in this situation. To overcome this phenomenon, this paper adopts the time-sharing sinusoidal PWM strategy to modify the load voltage. The time-sharing sinusoidal PWM method is shown in Fig. 3(a) [12]. Fig. 3(b) shows the corresponding switching patterns including time-sharing sinusoidal PWM strategy.

III Steady state analysis and design

The proposed system can be operated in continuous current mode (CCM) or discontinuous current mode (DCM) according to the load conditions. For simplicity, the CCM mode is adopted for the following analysis procedure.

A. Inverter stage operation principle

According to the proposed UPS shown in Fig. 1(b), there are two possible voltage waveforms in the dc bus, one is induced by the boost switch during the voltage sag, and the other is fed by the diode rectifier as the voltage swell takes place. If the source voltage is defined as follows:

$$V_S(t) = V_1 \sin(\omega_0 t + \theta_1) + \sum_{k=2}^{\infty} V_k \sin(k\omega_0 t + \theta_k) \quad , \qquad (1)$$

where $V_1 \sin(\omega_0 t + \theta_1)$ is the fundamental content, and $\sum_{k=2}^{\infty} V_k \sin(k\omega_0 t + \theta_k)$ is the total harmonics, then the dc bus voltage related to voltage sag and swell can be represented as the following equations, respectively:

$$V_{dc1}(t) = \frac{1}{(1-d)} |V_S(t)|, \qquad (2)$$

$$V_{dc2}(t) = |V_S(t)|. \qquad (3)$$

The inverter output voltage $V_0(t)$ can be represented as the product of dc bus voltage and switching function, and is obtained as follows:

$$V_O(t) = f(t) \cdot V_{dck}(t), \quad k = 1 or 2, \qquad (4)$$

where *f(t)* is the switching function decided by the control algorithm. When the inverter switches are operated at 60 Hz, the output voltage can be simply obtained as follows:

$$V_O(t) = V_{01}(t) = \frac{1}{(1-d)} V_S(t). \qquad (5)$$

Equation (2)-(5) shows the dc bus voltage is approximately equal to source voltage

when voltage swell occurred, and is approximately equal to normal load voltage ($\approx 110\sqrt{2}$ V) when voltage sag occurred, thus, the voltage stress is lower than the conventional constant dc bus voltage strategy. In addition, it also shows that the dc bus and load voltage have the same waveform shapes with the utility, it shows the other cause why the proposed system can have smaller values of input and output inductance than conventional structures. As the input inductor voltage is approximately equal to the difference between the utility and dc bus voltage when it is connected to the dc bus, and the output inductor voltage is approximately equal to the difference between dc bus and load voltage, thus, the same waveform shape means less value of voltage difference, resulting in a lower value of inductance. A similar conclusion about less voltage stress in the power switches can also be got in this way. Moreover, it can be seen that the load voltage regulation function is achieved by controlling the duty ratio of S_1 and/or (S_4, S_5), thus a large range of regulation capability can be expected.

When the inverter is switching in high frequency, two PWM switching strategies can be used here: termed the bipolar switching and unipolar switching. These strategies have the same fundamental frequency voltage, except that the dominant harmonic voltage centered around switching frequency disappeared for the latter strategy[11], resulting in a significantly low harmonic content, hence, adopted by this paper.

The switching function *f(t)* in accordance with the PWM strategy can be expressed by using Fourier series for a square wave, and is denoted as :

$$f(t) = A_0 + \sum_{n=1}^{\infty} (A_n \cos(n\omega_S t) + B_n \sin(n\varpi_S t)), \qquad (6)$$

where $\omega_S = \frac{2\pi}{T_s}$ ，and T_S is the PWM cycle.

Assuming the load current is continuous； the peak value of the carrier wave is 1; and let the carrier frequency be high enough related to the source frequency(which means the modulating signal can be treated as constant value in one switching cycle), then the amplitude of the square wave in this case is 1, and coefficients of A_0、A_n and B_n can be deduced as follows:

$$A_0 = \frac{1}{T_S}\int_0^{T_S} f(t)dt$$

$$= \frac{1}{T_S}(\int_0^{dT_S} 1dt + \int_{dT_S}^{T_S - dT_S} 0dt) = d \ , \qquad (7)$$

$$A_n = \frac{2}{T_S}\int_0^{T_S} f(t)\cos n\omega_S t dt$$

$$= \frac{\sin 2n\pi d}{n\pi} \ , \qquad (8)$$

$$B_n = \frac{2}{T_S}\int_0^{T_S} f(t)\sin n\omega_S t dt$$

$$= \frac{(1-\cos 2n\pi d)}{n\pi} \ , \qquad (9)$$

where d is the duty ratio, thus the switching function can be expressed as follows:

$$f(t) = d + \sum_{n=1}^{\infty} (A_n \cos(n\omega_S t) + B_n \sin(n\varpi_S t))$$

$$= d + \sum_{n=1}^{\infty} (C_n \sin(n\omega_S t + \psi)) \ , \qquad (10)$$

where

$$C_n = \sqrt{(A_n^{\ 2} + B_n^{\ 2})} = \frac{2}{n\pi} \sin n\pi d, \qquad (11)$$

$$\psi = \tan^{-1} \frac{A_n}{B_n} \ , \qquad (12)$$

By combining (1), （4）and （10）-(12), the inverter output voltage $V_{O2}(t)$ is given by

$$V_O(t) = V_{02}(t) = d \cdot V_S(t) + \sum_{k=1}^{\infty} \sum_{n=1}^{\infty} \frac{V_k \sin(nd\pi)}{n\pi} \cdot \qquad (13)$$

$$[\cos((n\omega_S - k\omega_0)t + (\psi - \theta_k)) + \cos((n\omega_S + k\omega_0)t + (\psi + \theta_k))].$$

Considering the fact, $w_S \rangle\rangle w_0$, and k is relatively small in practice [7], the effect of high order harmonics at load side can be neglected with the use of passive filters, therefore the load voltage can be simplified as follows:

$$V_{02}(t) = d \cdot V_S(t). \qquad (14)$$

From (14), it is clear that the load voltage and source input have the same shape of harmonic spectrum in low order range of harmonics.

B. Load voltage switching harmonics analysis

When the inverter is switching in high frequency, a passive filter is necessary for the switching harmonics. For a resistive load case shown in Fig. 4 (a), the load voltage V_L with respect to V_0 can be given by

$$\frac{V_L(s)}{V_o(S)} = \frac{R_L}{sL_r + (1 + s^2 L_r C_r) R_L}, \qquad (15)$$

If the source harmonics are neglected and assuming $\theta_1 = 0$, and $n\omega_s \pm \omega_0 \approx n\omega_s$, then $V_o(t)$ can be represented as follows:

$$V_o(t) = dV_S(t) + \sum_{n=1}^{\infty} \frac{2V_1 \sin(nd\pi)}{n\pi} \cos(n\omega_S t + \psi), \qquad (16)$$

Where the fundamental components V_{L1} and the switching harmonic component V_{Ln}, can be obtained by

$$V_{L1} = \frac{R_L dV_S}{\sqrt{\omega_0^{\ 2} L_r^{\ 2} + (1 - \omega_0^{\ 2} L_r C_r)^2 R_L^2}}, \qquad (17)$$

$$V_{Ln} \approx \frac{R_L V_{on}}{\sqrt{n^2 \omega_s^2 L_r^{\ 2} + [1 - n^2 \omega_s^2 L_r C_r]^2 R_L^2}}, \qquad (18)$$

where

$$V_{on}(t) = \frac{2V_1 \sin(nd\pi)}{n\pi}. \qquad (19)$$

For a practical filter design, the following conditions are usually satisfied [8]:

$$\omega_0 L_r << R_L, \text{ and } R_L << \frac{1}{\omega_0 C_r}. \quad (20)$$

Hence, the fundamental component V_{L1} can be approximated as follows:

$$V_{L1} \approx dV_S(t). \quad (21)$$

In Addition, it is usually held for $R_L << \omega_S L_r$, thus if a large switching frequency or a large output capacitor is adopted, resulting in $\frac{1}{\omega_S C_r} << R_L$, then (18) can be simplified as follows:

$$V_{Ln} \approx \frac{V_{on}}{n^2 \omega_s^2 L_r C_r}. \quad (22)$$

The above equation shows the switching harmonic component V_{Ln} is independent on the load resistance, and can be easily filtered out with small parameters of L_r and C_r.

Similarly, the inductor current I_R with respect to PWM voltage V_0 is given by

$$\frac{I_R(s)}{V_o(S)} = \frac{1 + sC_r R_L}{sL_r + (1 + s^2 L_r C_r) R_L}, \quad (23)$$

where the fundamental components I_{R1} and the harmonic components I_{Rn}, are given by

$$I_{R1} = \frac{\sqrt{1 + \omega_0^2 C_r^2 R_L^2}\, dV_S}{\sqrt{\omega_0^2 L_r^2 + (1 - \omega_0^2 L_r C_r)^2 R_L^2}} = \frac{dV_S}{R_L}, \quad (24)$$

$$I_{Rn} \approx \frac{\sqrt{1 + n^2 \omega_S^2 C_r^2 R_L^2}\, V_{on}}{\sqrt{n^2 \omega_S^2 L_r^2 + (1 - n^2 \omega_S^2 L_r C_r)^2 R_L^2}} \approx \frac{V_{on}}{n \omega_S L_r}. \quad (25)$$

The above equation shows that the parameter L_r has a significant role for filtering the switching harmonic current. By combining (22), (25), the parameters of L_r and C_r can be determined.

C. Input switching harmonics analysis

The input switching harmonics are mainly decided by the rectifier input voltage V_{AB}. It is approximated to zero when the boost switch is turned on, and is approximated to V_{dc} when the boost switch is turned off. Thus, V_{AB} can be expressed as follows:

$$V_{AB}(t) = g(t) \cdot V_S(t), \quad (26)$$

where *g(t)* is the switching function, which can be calculated using Fourier series for a square wave, and is denoted as :

$$g(t) = D_0 + \sum_{n=1}^{\infty} (D_n \cos(n\omega_s t) + E_n \sin(n\varpi_s t)). \quad (27)$$

Here, the amplitude of the square wave is $\frac{1}{(1-d)}$, and coefficients of D_0, D_n and E_n can be deduced as follows:

$$D_0 = \frac{1}{T_S}\int_0^{T_S} g(t)dt$$

$$= \frac{1}{T_S}(\int_0^{d.T_S} 0dt + \int_{dT_S}^{T_S - d.T_S} \frac{1}{1-d}dt) = 1, \qquad (28)$$

$$D_n = \frac{2}{T_S}\int_0^{T_S} f(t)\cos n\omega_S t dt$$

$$= \frac{-\frac{1}{(1-d)}\sin 2n\pi d}{n\pi}, \qquad (29)$$

$$E_n = \frac{2}{T_S}\int_0^{T_S} g(t)\sin n\omega_S t dt$$

$$= \frac{-\frac{1}{(1-d)}(1-\cos 2n\pi d)}{n\pi}, \qquad (30)$$

then the switching function can be given by

$$g(t) = 1 + \sum_{n=1}^{\infty}(F_n \sin(n\omega_S t + \vartheta)) \ , \qquad (31)$$

where

$$Fn = \sqrt{(D_n^{\ 2} + E_n^{\ 2})} = \frac{2\frac{1}{(1-d)}}{n\pi}\sin n\pi d, \qquad (32)$$

$$\vartheta = (\pi + \tan^{-1}\frac{|A_n|}{|B_n|}) \ , \qquad (33)$$

By combining (26) and (31)-(33), $V_{AB}(t)$ can be expressed as follows:：

$$V_{AB}(t) = V_S(t) + \sum_{k=1}^{\infty}\sum_{n=1}^{\infty}\frac{V_k \sin(nd\pi)}{n\pi}\cdot \qquad (34)$$

$$[\cos((n\omega_s - k\omega_0)t + (\psi - \theta_k)) + \cos((n\omega_s + k\omega_0)t + (\psi + \theta_k))]$$

Neglecting the source harmonics and assuming $\theta_1 = 0$, $n\omega_s \pm \omega_0 \approx n\omega_s$, $V_{AB}(t)$ can be simplified as follows:

$$V_{AB}(t) = V_1(t) + \sum_{n=1}^{\infty}\frac{2V_1 \sin(nd\pi)}{n\pi}\cos(n\omega_S t + \psi).$$

$$= V_1(t) + \sum_{n=1}^{\infty}V_{on}\cos(n\omega_S t + \psi). \qquad (35)$$

Fig 4(b) shows the input equivalent circuit for the switching harmonic V_{on}, where L_S denoted the input inductor. From Fig. 4(b), the harmonic current can be obtained as follows:

$$i_{sk} \approx \frac{V_{on}}{n\omega_S L_S}. \qquad (36)$$

D. DC bus capacitance design

For the proposed topology, the load power is fed directly by the utility when the load is resistive. However, when the load current is leading or lagging the load voltage, it is necessary to give a path for the load current flow. This is done by the dc bus capacitor, which carriers the load current as the voltage and current have opposite signs. The size of the dc bus capacitor can be estimated by calculating the power flow in this interval [10]. Suppose the load is given by

$$Z_{\text{Load}}(\varphi) = \frac{V_L}{I_L}\angle\varphi, \\ = R_{Lrad} + j\omega_0 L_{load}. \qquad (37)$$

$$R_{load} = \frac{V_L}{I_L}\cos(\varphi), \qquad (38)$$

$$L_{load} = \frac{1}{\omega_0}\frac{V_L}{I_L}\sin(\varphi).$$

If the load voltage and current are sinusoidal, then the load current at the point, $\omega_0 t = \pi$, (where the load voltage crosses zero) is given by

$$I_{L0} = \hat{I}_L \sin(\pi - \varphi) = \hat{I}_L \sin(\varphi), \qquad (39)$$

where $\hat{I}_L$ is the peak value of load current. The load current will cross zero for the instant time of $t_0 = \frac{\varphi}{2\pi}\cdot T_0 = \frac{\varphi}{\omega_0}$. Based on the energy balance concept, the energy stored in the load inductor will be released to the dc bus capacitor or dissipated in the load resistor. The related equation can be given by

$$\frac{1}{2}C_{dc}(V_{dc}(\frac{\varphi}{\omega_0}))^2 + R_{load}\int_0^{\frac{\varphi}{\omega_0}}(\hat{I}_L \sin(\omega_0 t))^2 dt = \frac{1}{2}L_{load}(I_{L0})^2. \qquad (40)$$

Thus, the capacitance of the dc bus is given by

$$C_{dc} = \frac{L_{load}(I_{L0})^2 - R\hat{I}_L^2 \cdot \frac{-\cos\varphi\sin\varphi + \varphi}{\omega_0}}{(V_{dc}(\frac{\varphi}{\omega_0}))^2}. \qquad (41)$$

The above equation shows that the larger the L_{load} (so that the lower the load power factor), the larger the dc bus capacitor. For a case of $Z_{\text{Load}}(\varphi) = 12\angle\varphi$, then the corresponding dc bus voltage $V_{dc}(\frac{\varphi}{\omega_0})$ due to different dc bus capacitors can be shown as follows:

$C_{dc} = 2\mu F,$

$$\varphi = 10^0 \to V_{dc}(\frac{\varphi}{\omega_0}) = 70V, \quad \varphi = 20^0 \to V_{dc}(\frac{\varphi}{\omega_0}) = 198V, \quad \varphi = 30^0 \to V_{dc}(\frac{\varphi}{\omega_0}) = 353V,$$

$C_{dc} = 20\mu F,$

$$\varphi = 10^0 \rightarrow V_{dc}(\frac{\varphi}{\omega_0}) = 22V, \quad \varphi = 20^0 \rightarrow V_{dc}(\frac{\varphi}{\omega_0}) = 63V, \quad \varphi = 30^0 \rightarrow V_{dc}(\frac{\varphi}{\omega_0}) = 112V.$$

It shows a large dc bus capacitor results in a small dc bus voltage, however, too large a dc bus capacitor will destroy the input power factor and the dc bus voltage waveform shape will become constant, thus a tradeoff should be made between the dc capacitor value and bus voltage.

E. Load voltage control loop

Fig. 5(a) shows the control block diagram of the proposed system. It is mainly composed of a zero-crossing detector, source voltage and current detectors, load voltage detector, a PI controller, a PWM/60Hz control algorithm according to Fig. 2, and a PWM/60Hz pulse generator. The PI controller is used to regulate the load voltage to ensure the command is followed. Fig. 5(b) shows the load voltage control block diagram, where V_L denotes the amplitude of the load voltage, K_{PT} denotes the turn ratio of the potential transformer, and K_{rec} denotes the gain of the precision rectifier, $G_{NF}(s)$ represents the notch filter, and can be shown as

$$G_{NF}(s) = \frac{s^2 + \omega^2_{NF}}{s^2 + \frac{\omega_{NF}}{Q}s + \omega^2_{NF}} \qquad (42)$$

where ω_{NF} denotes the notch frequency, and Q denotes the quality factor. The quality factor can have a significant effect on the ripple rejection capability, and a small value of Q can have a significant notching effect. However, too small is not recommended because it is adverse to the dc voltage regulator, thus, a trade-off must be made. In this paper, the control parameters are selected as follows: K_P =2, K_i =50, K_{PT} =3/110, ω_{NF} =2*3.14*120, Q$\cong$ 10.

IV. Experimental results

A prototype of *1 kVA* UPS is constructed to verify the proposed idea. System parameters are selected as follows: V_S=*110*V_{rms} nominally; V_B=*48V*, switching frequency =*30 kHz; L_S=0.2mH, L_r=0.2mH; C_r=2.2uF; C_{dc}=2.2uF.*

Fig. 6 shows the experimental results for a resistive load of R_L=12Ω, when the system is operated in the normal mode, including three types of source voltage (V_S=*90*V_{rms}, *110*V_{rms}, *130*V_{rms}), Fig. 6(a) shows the source voltage and the corresponding load voltage for the voltage sag case. It shows that the source voltage has been boosted to the desired level. Fig. 6(b) shows the normal source voltage situation, where the source and load voltage have nearly the same amplitude. Fig. 6(c) shows the source voltage and the corresponding load voltage for voltage swell occurred, there the proposed inverter has decreased the source voltage amplitude.

Fig. 7 shows the system performance in the load case of R_L=12Ω, when voltage sag occurred (V_S=*90*V_{rms}). Fig. 7(a) shows the source voltage and current. It shows the source current has a high quality of waveform shape. Fig. 7(b) shows the load voltage and

current. It shows the load voltage has been boosted to the desired level, and has also a high quality of waveform shape. Fig. 7(c) shows the corresponding DC bus voltage. It shows the proposed system has an excellent performance in this type of load.

Fig. 8 shows the experimental results when the proposed system is operated in RL load condition, where R=12 Ω, L= 3mH ($Z \simeq 12, \quad \varphi = 5.4^0 \rightarrow V_{dc}(\frac{\varphi}{\omega_0}) \simeq 28V$). Fig. 8(a) shows the source voltage and current. It shows a current distortion occurred. Fig. 8(b) shows the load voltage and current. It shows a similar waveform shape presented in the load current. Fig. 8(c) shows the corresponding DC bus voltage. It shows the source current is mainly dependent on the load current since most of the energy is directly supplied from the utility source through the proposed inverter stage to the load. Fig. 8(c) also shows a different waveform shape from Fig. 7(c), where $V_{dc}(\frac{\varphi}{\omega_0}) \simeq 28V$ can be observed in this figure.

Fig. 9(a) shows the transient responses of the load voltage and current due to a load change, where it is changed from 100 Ω to 12Ω. It shows the proposed inverter can maintain the load voltage in accordance with the load change. Fig. 9(b) shows the relationship between the efficiency and different source voltages in normal operation mode, where R=12Ω, it shows the proposed system has a higher efficiency than conventional two-stage based structures. Fig. 9(c) shows the corresponding efficiency due to different load capacity which is also obtained in the normal operation mode, where V_S=85V. It shows a similar result as Fig. 9(b). The efficiency in the backup mode is lower than the case in the normal operation mode, as it faces the battery which is with different waveform shape with the desired dc bus voltage pattern.

Figure 10 shows the experimental results of a diode rectifier load. The rectifier load consists of a resistor of 36Ω in parallel with a capacitor of 1200 μF, and an inductor of 3mH added in series on the AC side to improve the current waveform. Figure 10(a) shows the source voltage and current. Fig. 10(b) shows the load voltage and load current. Figure 10(c) shows the corresponding DC bus voltage. In this case, one can see that the source current has a similar waveform shape to the load current. It means the proposed system can not have the function of correction the load harmonics, thus it is not suitable in the situation where the power factor correction function is required. Moreover, as the limitation of the small dc bus capacitance, it can not have the capability to supply burst current into the rectifier, thus a load voltage distortion occurred in this structure.

Fig. 11 shows the experimental results in the backup mode, where R=12Ω, and the inverter stage is switched in 60 Hz. Fig. 11(a) shows the DC bus voltage. Fig. 11(b) shows the corresponding load voltage. It shows the load voltage is boosted to the desired level, and the batteries are maintaining the load voltage. However, it is rich in harmonics. Fig. 11(c) shows the spectrum of the load voltage harmonics. It shows the load voltage contains large values of harmonic, and the total harmonic distortion is about 20.7%.

Fig. 12 shows a similar result in the backup mode, where the time-sharing sinusoidal PWM method is adopted. Fig. 12(a) shows the corresponding DC bus voltage. Fig. 12(b) shows the load voltage. Fig. 12(c) shows the load voltage harmonics. It shows the voltage harmonics have been reduced effectively, where the total harmonic distortion is about 6.8%.

V. Conclusion

In this paper, a compact line-interactive UPS has been described. A novel and effective control strategy has been verified for the compensation of source voltage fluctuations in the normal mode, and it can also be used in the backup mode. It provides benefits including:

1) A large regulation range to compensate the source voltage swells and sags.
2) Small values of input inductor, output inductor and dc bus capacitor.
3) A simple control algorithm for the load voltage regulator.
4) High efficiency due to the proposed switching strategies.
5) High power density and low cost.

Prototype experiments including different loads have demonstrated that the proposed method is effective. It presents the proposed structure is suitable for the resistive load type, but has limited ability to handle the load with low power factor. However, a compact structure consisted of small passive power elements shows the developed system to be valuable for the uninterruptible power supply and ac voltage regulator applications.

VI. Acknowledgments

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VII. References

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Figure captions

Fig. 1. The circuit diagrams of the proposed single-phase line-interactive UPS with small dc bus capacitor, (a) one-diode type, (b) two-diode type.

Fig. 2. The proposed switching patterns for different operation conditions, (a) voltage sag condition, (b) voltage swell condition, (c) backup mode condition.

Fig. 3(a). The time-sharing sinusoidal PWM method.
Fig. 3(b). The corresponding switching pattern including time-sharing sinusoidal PWM strategy used in backup mode.

Fig. 4(a). The harmonics equivalent circuit of the inverter stage.
Fig. 4(b). The harmonics equivalent circuit of the rectifier stage.

Fig. 5(a). The DSP based control block diagram of the proposed system.
Fig. 5(b). The control block diagram of the load voltage regulator

Fig. 6. The experimental results for three cases of source voltage, (a) the source voltage and corresponding load voltage for voltage sag situation, (b) the source voltage and corresponding load voltage for normal voltage situation, (c) the source voltage and corresponding load voltage for voltage swell situation.

Fig. 7. The experimental results in the R load condition, (a) the source voltage and current, (b) the load voltage and current. (c) the corresponding DC bus voltage

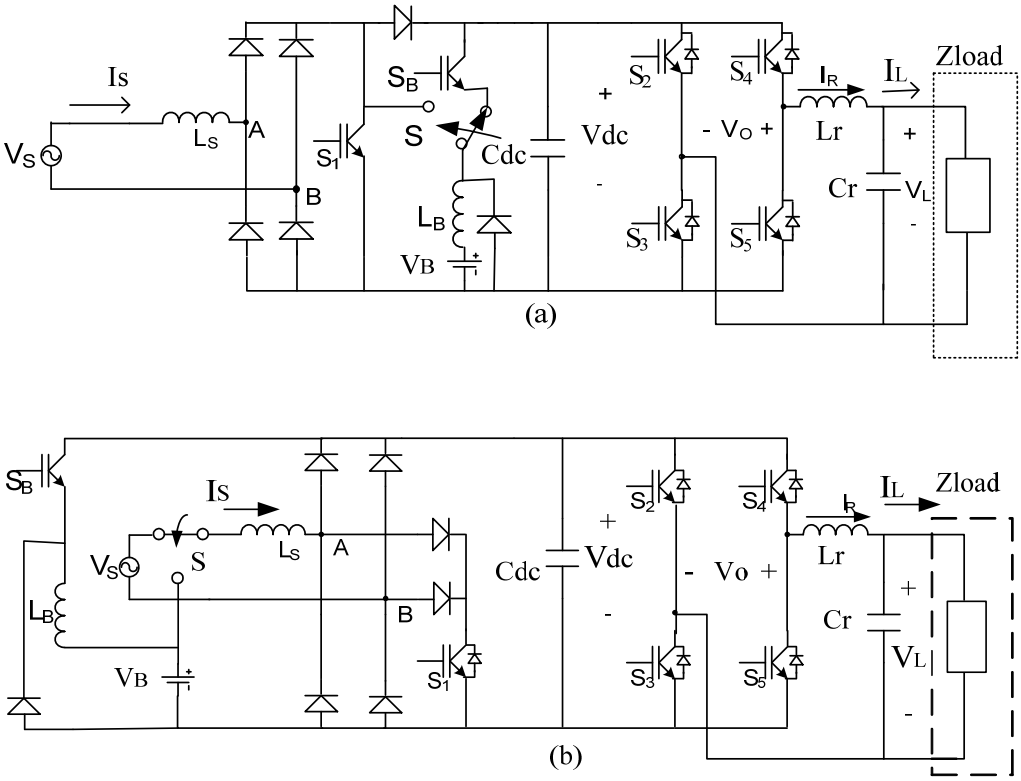
Fig. 8. The experimental results in the RL load condition, (a) the source voltage and current, (b) the load voltage and current. (c) the corresponding DC bus voltage.

Fig. 9(a). The system performance due to a load change (100Ω to 12Ω).
Fig. 9(b). The corresponding efficiency due to different source voltages (R=12Ω).
Fig. 9(c) The corresponding efficiency due to different load capacities (V_S=85V).

Fig. 10. The experimental results for a diode rectifier load, (a) the source voltage and current, (b) the load voltage and current, (c) the corresponding DC bus voltage.

Fig. 11. The experimental results in the backup mode, where the inverter stage is switched in 60 Hz mode, (a) the corresponding DC bus voltage, (b) the corresponding load voltage,, (c) load voltage harmonic spectrum.

Fig. 12. The experimental results in the backup mode, where the time-sharing sinusoidal PWM method is adopted, (a) load voltage and load current, (b) the corresponding DC bus voltage, (c) load voltage harmonic spectrum.



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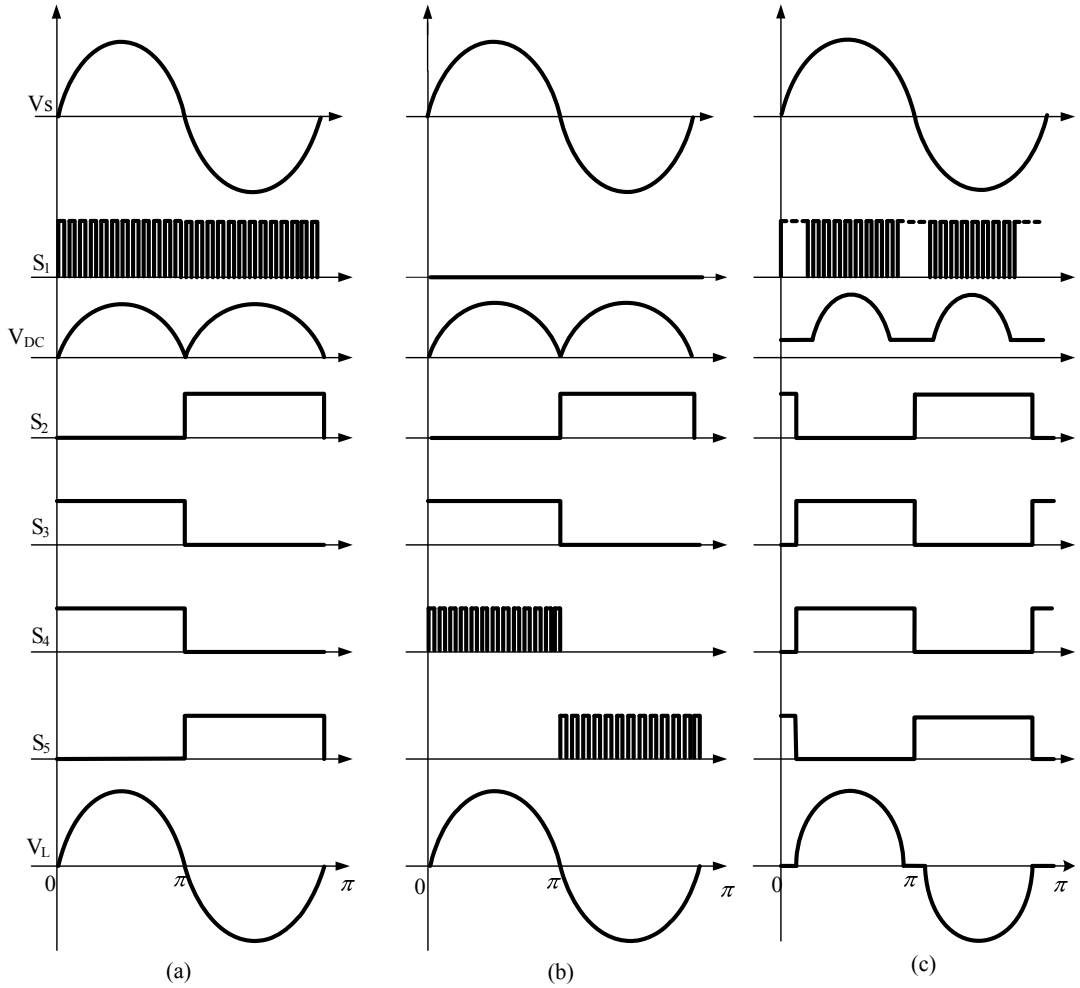

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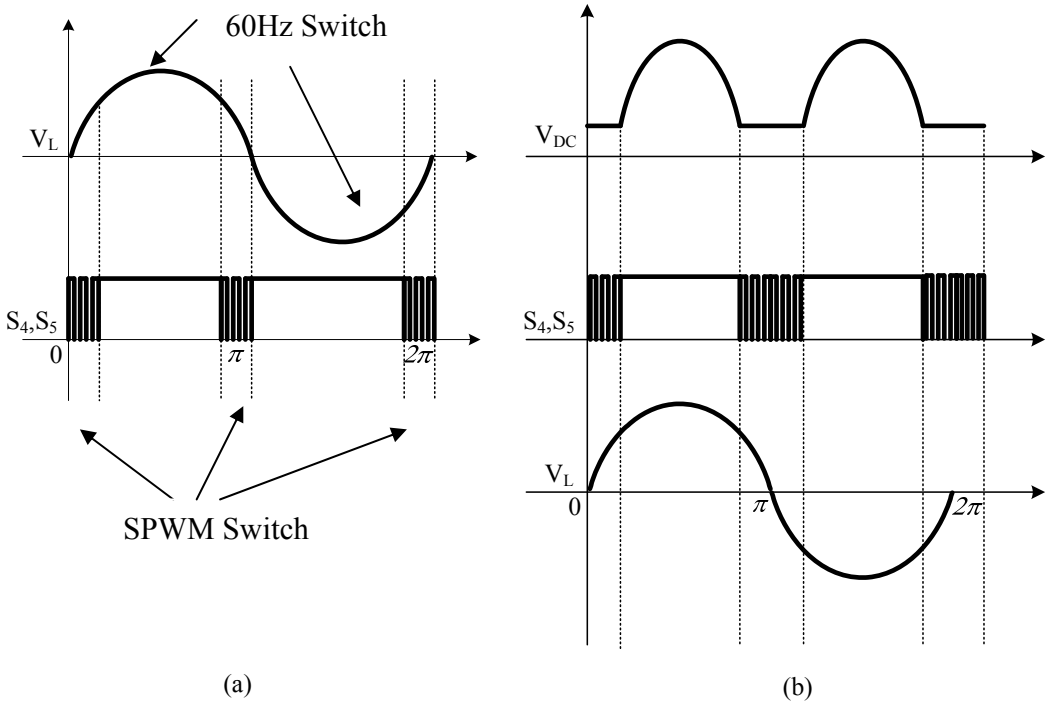

Fig. 3(a). The time-sharing sinusoidal PWM method.
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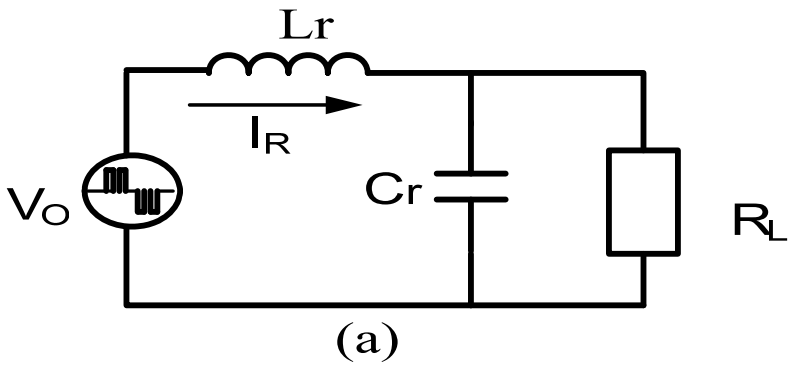
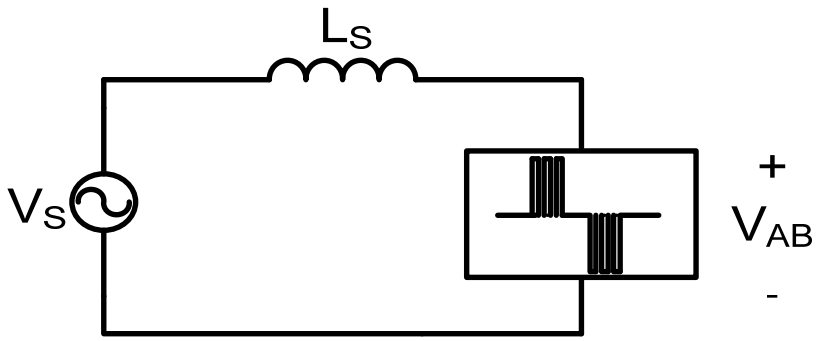


(a)



(b)

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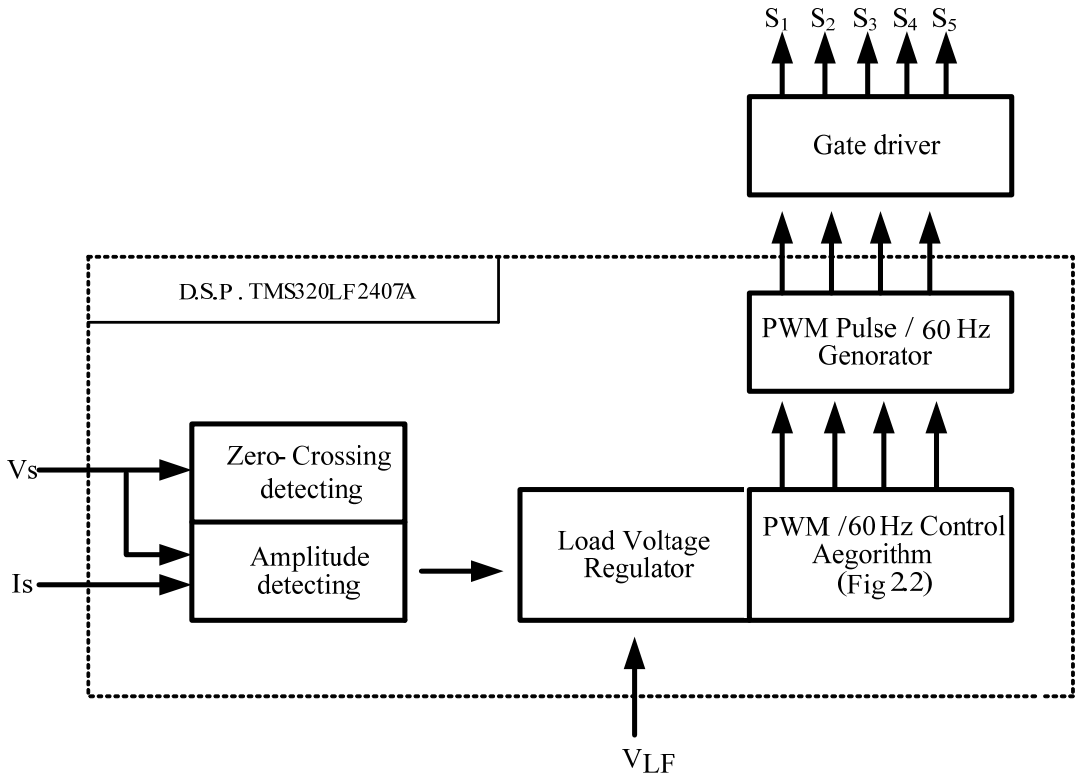


Fig. 5(a). The DSP based control block diagram of the proposed system.

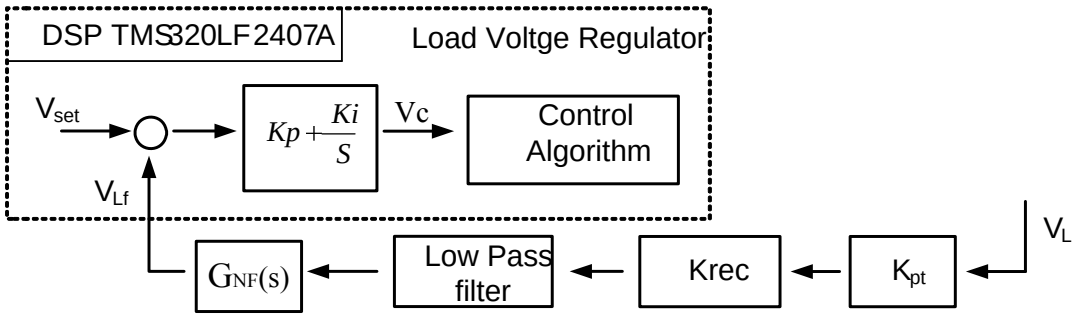
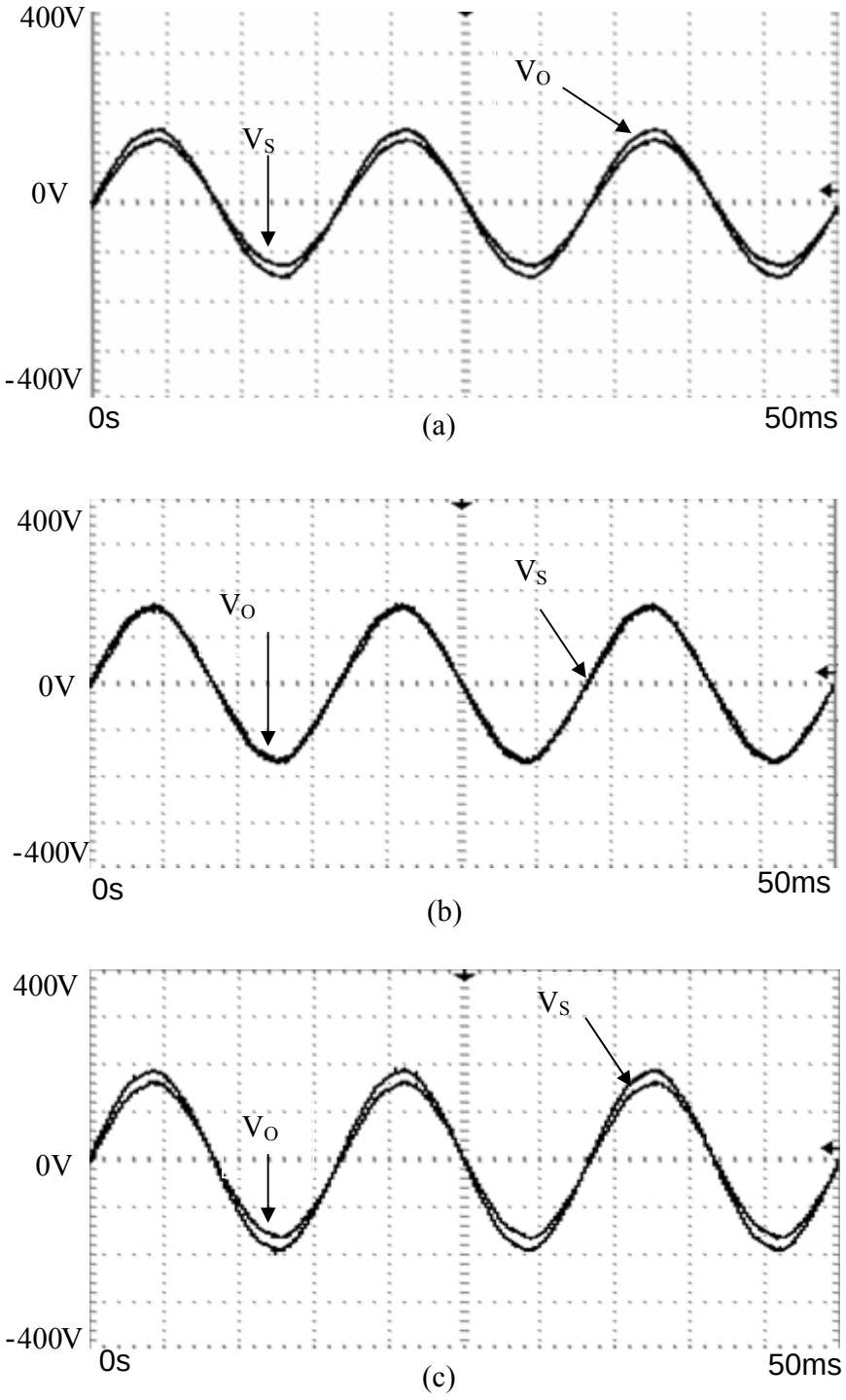


Fig. 5(b). The control block diagram of the load voltage regulator



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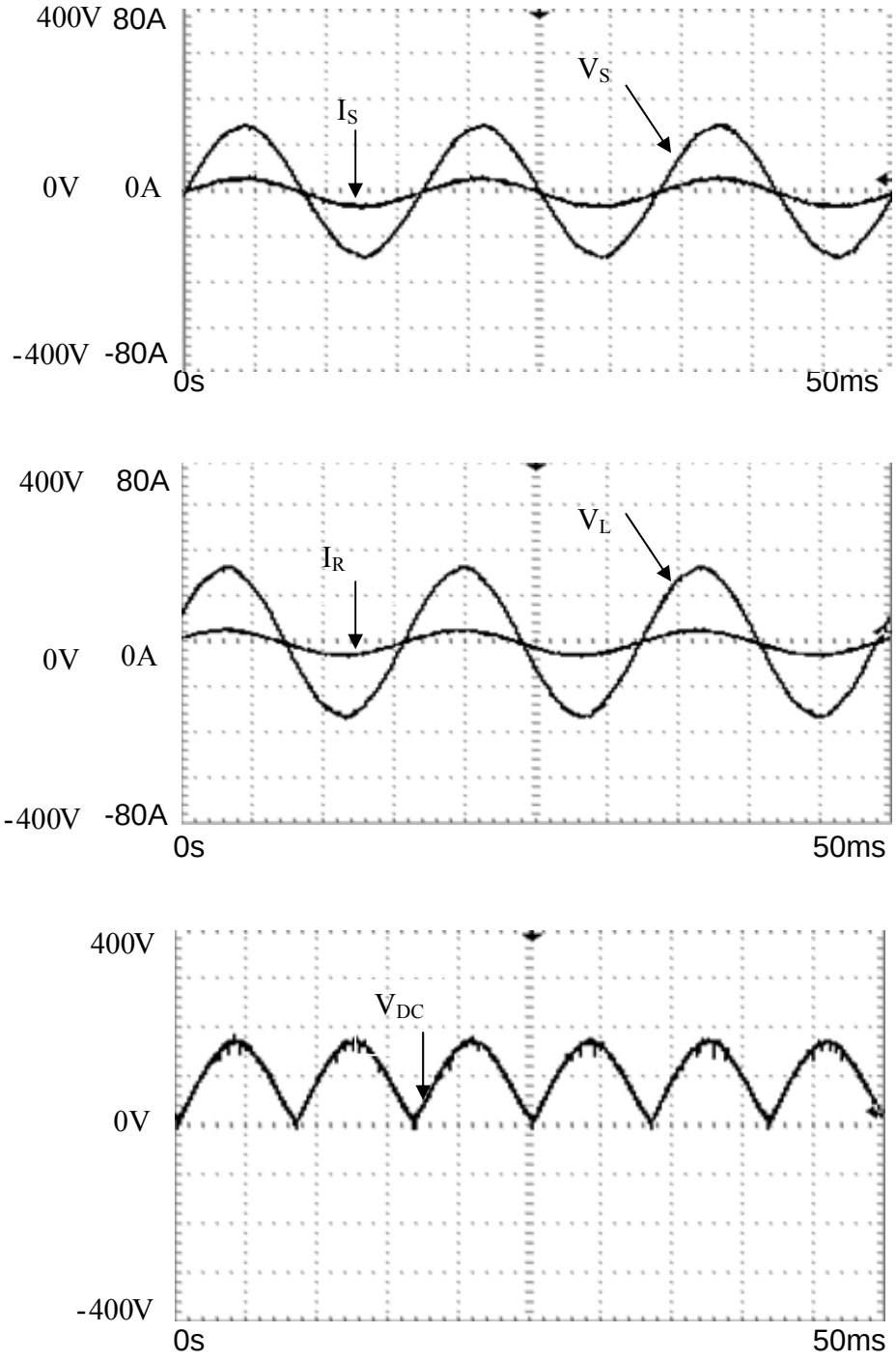

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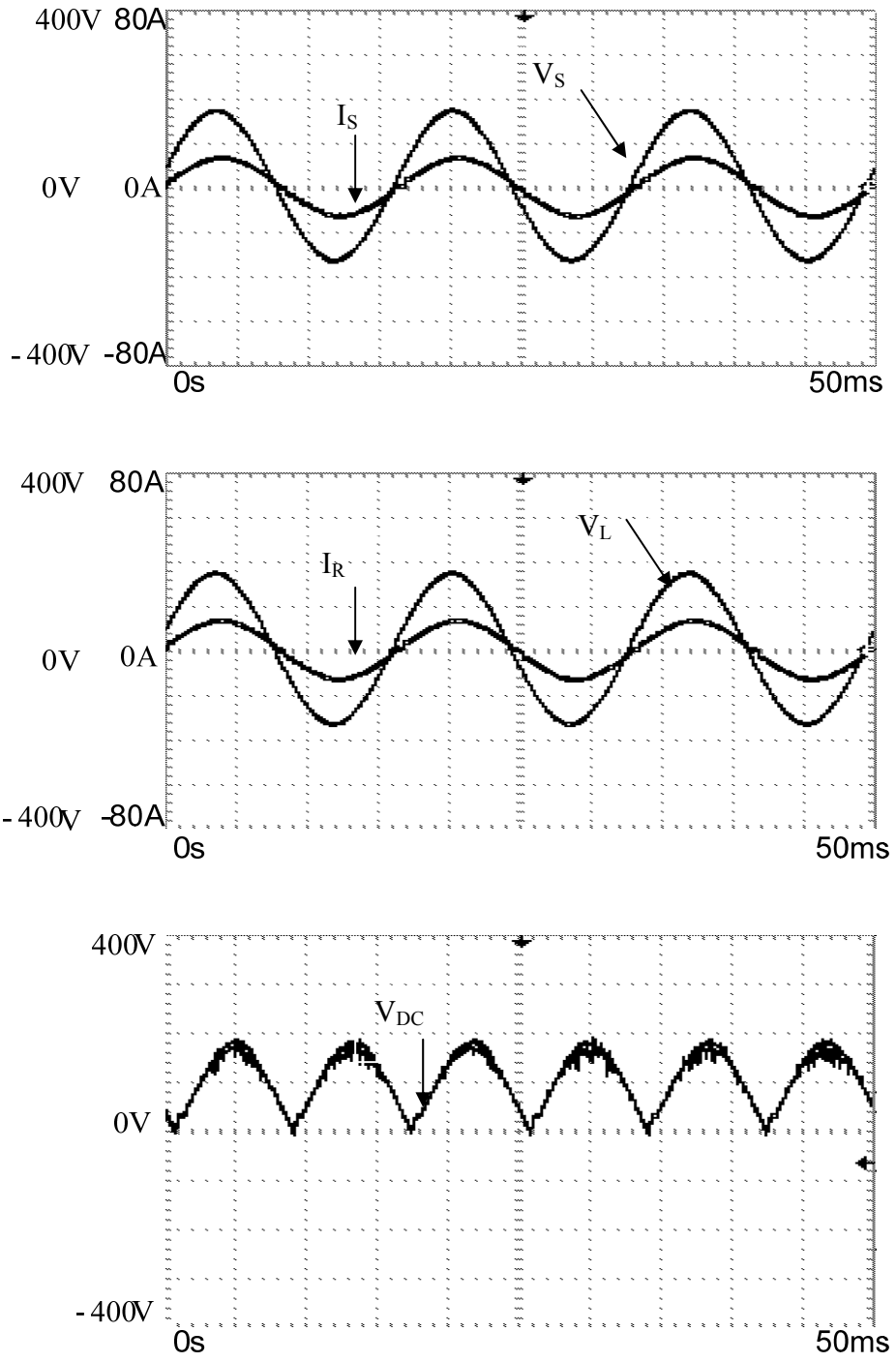

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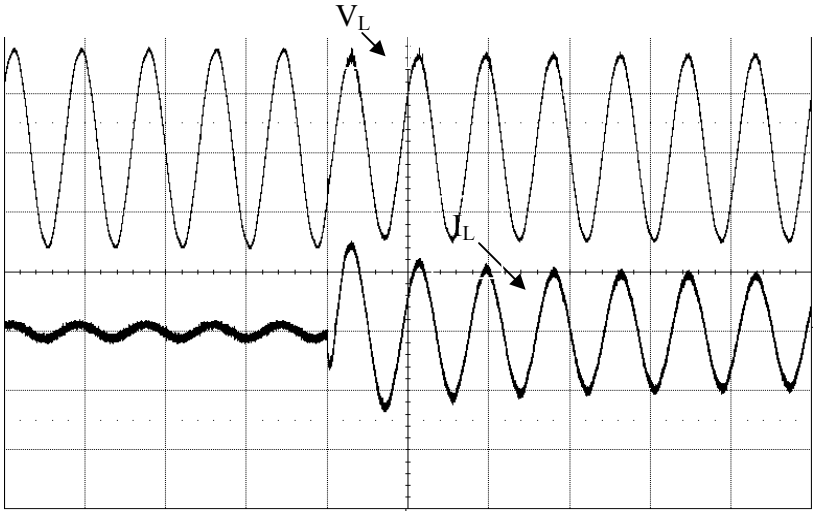


V: 100V/ div,I: 10A/ div

Fig. 9(a). The system performance due to a load change (100Ω to 12Ω).

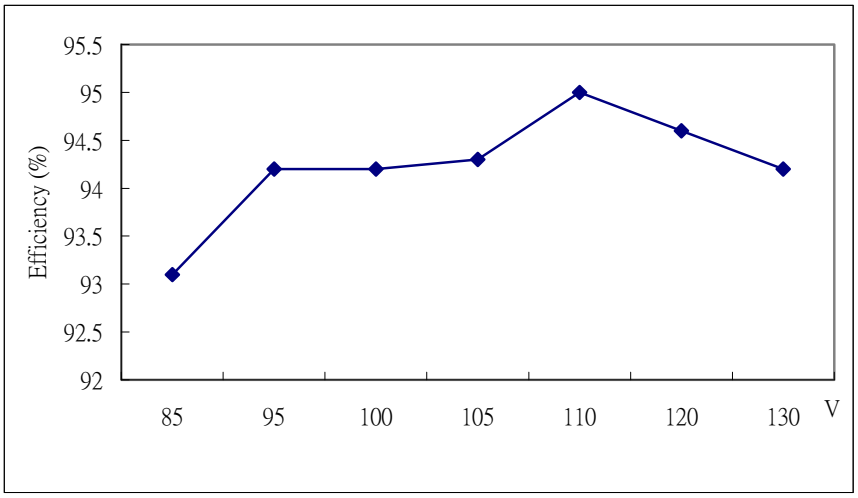


Fig. 9(b). The corresponding efficiency due to different source voltages (R=12Ω).

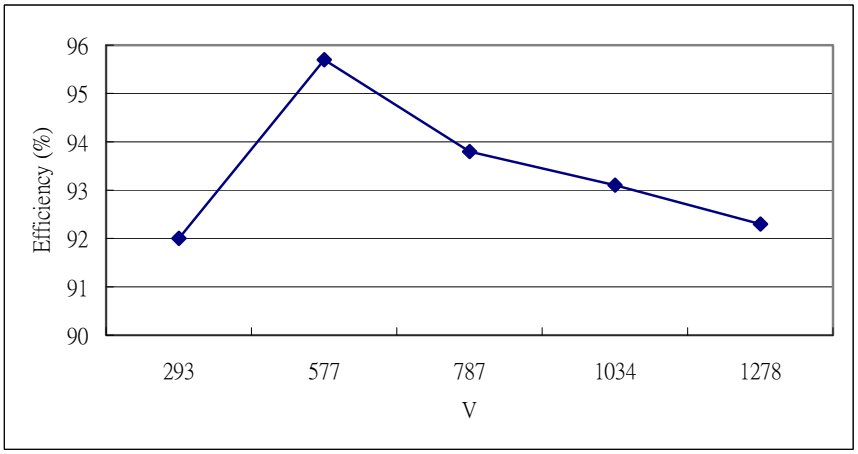
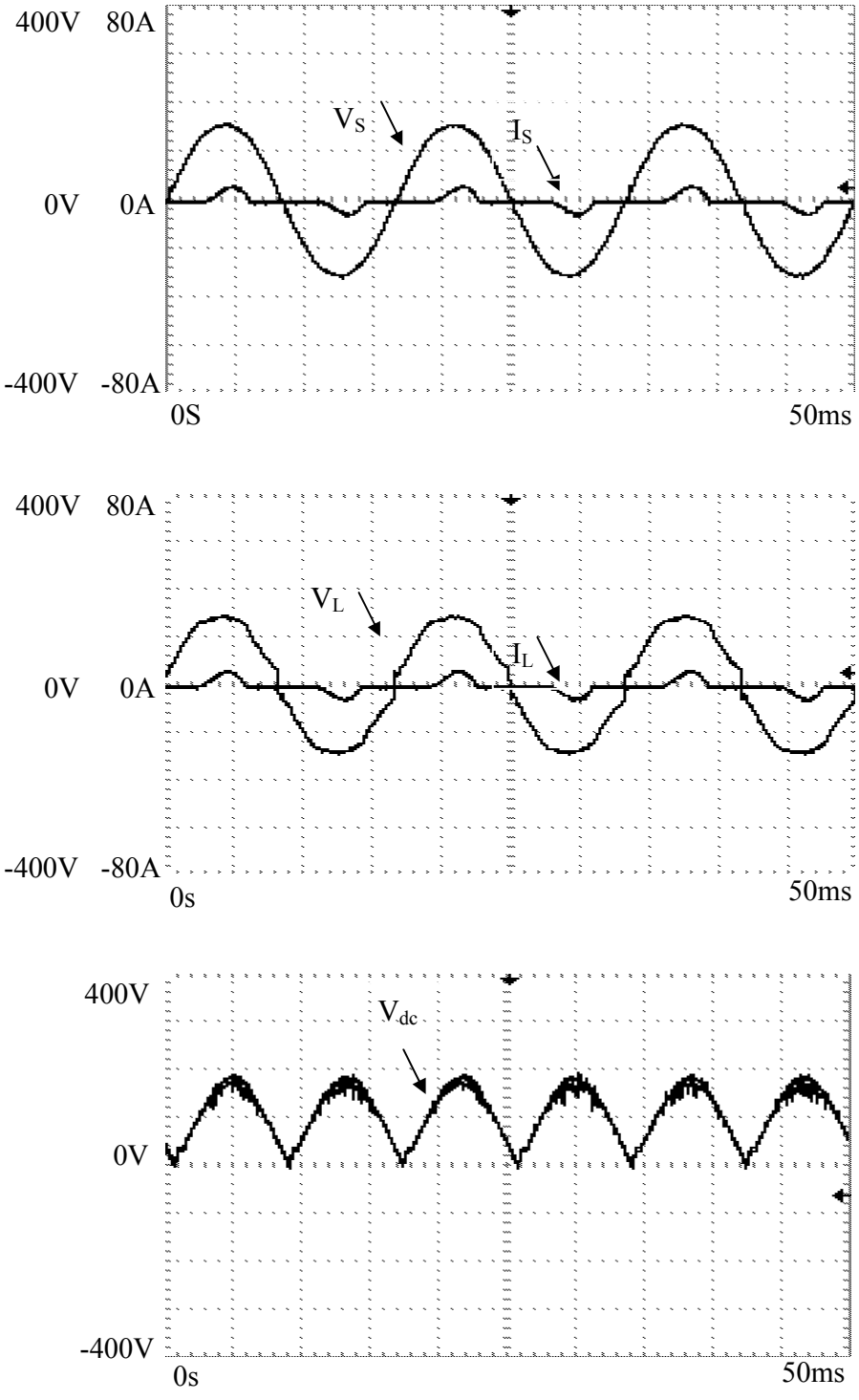


Fig. 9(c) The corresponding efficiency due to different load capacities (V_S=85V).



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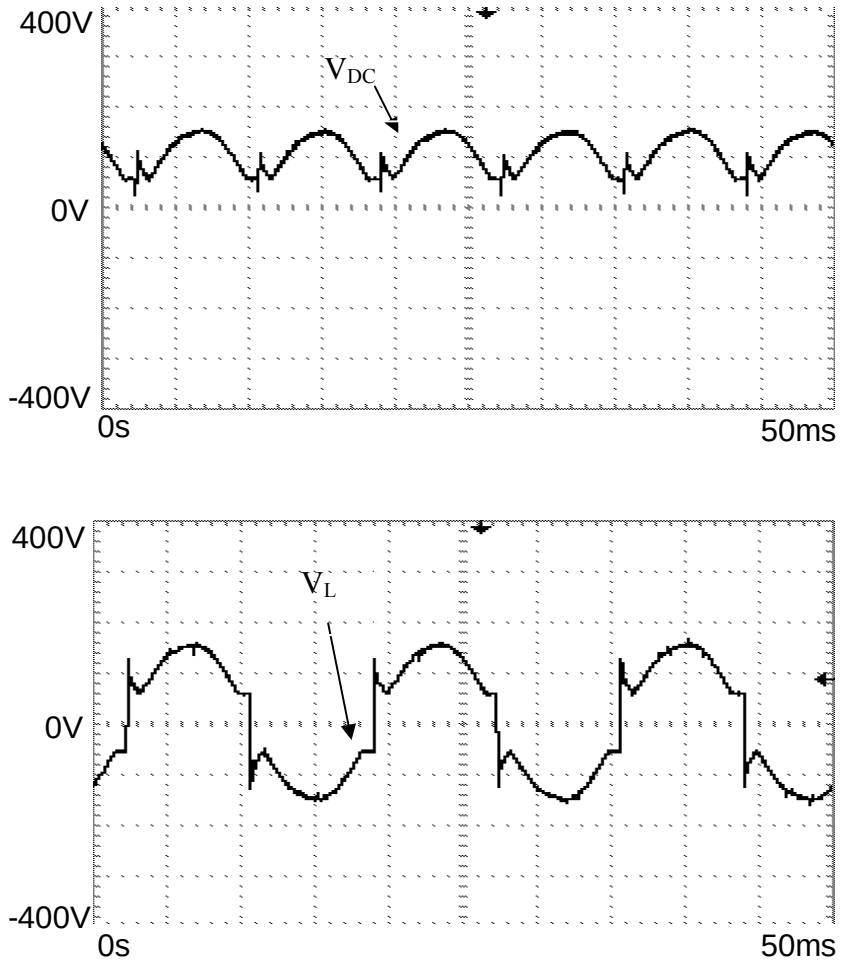

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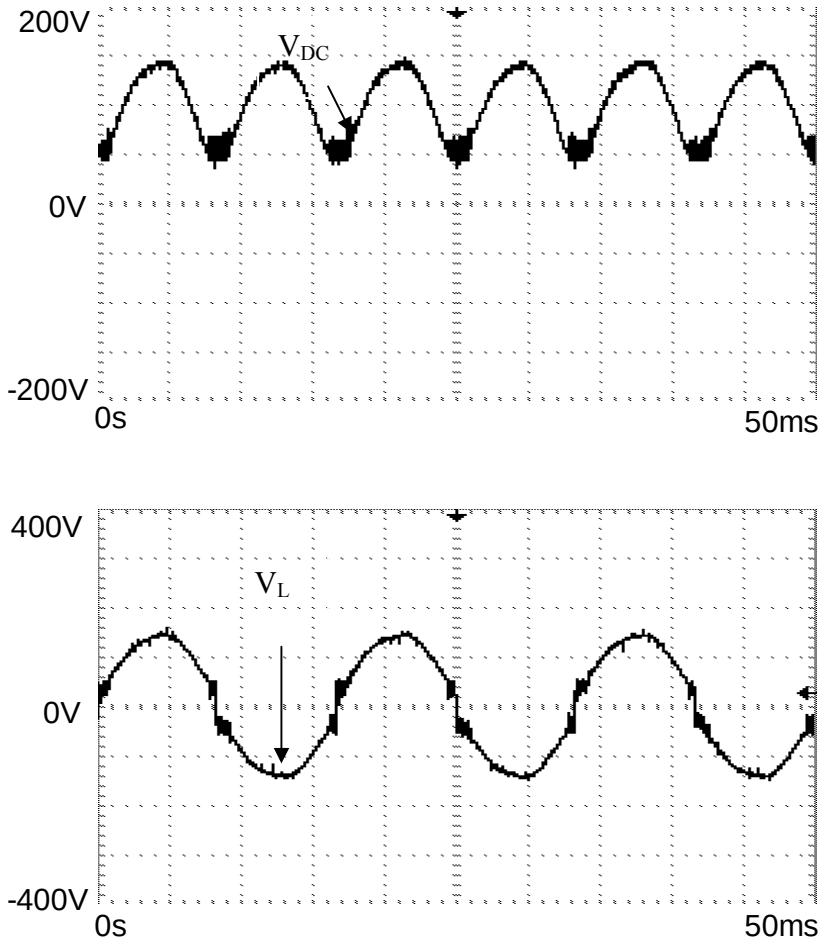

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