RELIABILITY PREDICTION

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Reliability prediction is the statistical art of determining a value of time over which a device will function. It is closely related to thermal performance, and the primary failure mode in electronics is thermal induced. In this section the MIL-HDBK-217 is introduced, which establishes uniform methods for predicting the reliability of electronic equipment and systems. The MIL-HDBK-217 procedure provide models for both a parts-count analysis and for a stress analysis. The parts-count model assumes typical operating parameters for a component and is used when most of its operating parameters are unknown. The stress model requires a detailed analysis of all of the parameters on which the component failure-rate depends.

9.1 **Device Models**

The constant failure-rate reliability model is used by all of the reliability prediction procedures here. With this model, the failure rate of any higher level assembly (assuming a series logic diagram) is the sum of the failure rates of its constituent components, but it does not include interconnects, stress interactions, solder joints, etc.

The models for microelectronics integration circuits in each of the reliability prediction procedures are

$\lambda = \Pi_Q(C_1\Pi_T\Pi_V + C_2\Pi_E)\Pi_L$ for stress model

$\lambda = \lambda_G\Pi_Q\Pi_L$ for parts-count model

where

Π_Q : quality factor.
C_1 & C_2 : failure rate constants.
Π_T : temperature acceleration factor.
Π_V : voltage-stress factor.
Π_E : environmental factor.
Π_L : device or process learning factor.
λ_G : generic or average failure rate.

9.2 **Failure Rate Constants**

C_1 is the circuit complexity failure-rate factor which is based on the circuit technology, and is the package complexity failure-rate factor. Circuit complexity is measured the number of the bits for digital devices, transistors for linear devices, and gate for logic devices. C_1 is tabulated in the procedure for various device types and is generally proportional to the square root of the complexity. For small DRAMs (less than 16K bits), C_1 = 0.025; for DRAMs of 256K to 1M bits, C_1 = 0.2. For monolithic bipolar and MOS linear devices, C_1 is 0.01 for devices of less than 100 transistors, and 0.04 for devices of 300 to 100 transistors.

C_2 depends on the package type and package pin count. It is calculated by the following equations:

Hermetic DIPs with solder or weld seals, Leadless Chip Carrier(LCC)	$C_2 = 2.8\times10^{-4}\times N_p^{1.08}$
Hermetic DIPs with glass seals	$C_2 = 9.0\times10^{-5}\times N_p^{1.51}$
Non-hermetic DIPs	$C_2 = 2.0\times10^{-5}\times N_p^{1.23}$
Hermitic Flatpacks	$C_2 = 3.0\times10^{-5}\times N_p^{1.82}$
Hermetic Cans	$C_2 = 3.0\times10^{-5}\times N_p^{2.01}$

where N_p is the number of pins on a device package which are connected to some substrate location.

9.3 **Quality Factor**

Component quality is generally determined by the controls and the inspections and tests used in the manufacturing process. The quality factor, Π_Q, expresses the relationship of component quality to the failure rate. The values of Π_Q are 0.25, 0.75, 1, 2, 5, 10, and 20 respective to seven different quality levels, S, S-1, B, B-1, B-2, D, D-1.

S and S-1 quality levels are intended for devices having very high reliability requirements such as when a failure could result in the loss of a life or an expensive satellite. These devices must be procured in full accordance with MIL-M-38510, Class S requirements which require 100% inspection or testing of devices for most tests, and an entire lot is rejected if more than a stated fraction, typically 5% or 10%, of the devices fail.

MIL-M-38510 requirements for class B are less stringent than class S. For example, devices in class S require 240 hours of burn-in at 125 ^{o}C whereas those in class B requires

only 160 hours of burn-in. Classes B-1 and B-2 allow further leeway in the test procedures.

Class D is used for hermetically sealed parts with normal reliability screening and manufacturer's quality assurance practices. Nonhermetic parts encapsulated with organic material must be subjected to 160 hours burn-in at 125 ^{o}C, 10 temperature cycles(-55 ^{o}C to 125 ^{o}C) with end point electricals and high temperature continuity test at 100 ^{o}C. Class D-1 is used for non-hermetic, commercial parts.

9.4 **Environment Factor**

The environmental factor, Π_E , accounts for the effects of environmental stresses on the device reliability. Each of the reliability prediction procedures lists typical environments within their range of applicability and gives corresponding value for Π_E. There are 27 different environment shown as following:

Environment	Symbol	Π_E	Environment	Symbol	Π_E
Ground, Benigh	G_B	0.38	Airborne, Inhabited, Attack	A_{IA}	4.0
Ground, Missile Silo	G_{MS}	0.65	Airborne, Inhabited, Fighter	A_{IF}	6.0
Ground, Fixed	G_F	2.5	Airborne, Unihabited, Cargo	A_{UC}	3.0
Ground, Mobile	G_M	4.2	Airborne, Unihabited, Trainer	A_{UT}	4.0
Manpack	M_P	3.8	Airborne, Unihabited, Bomber	A_{UB}	7.5
Naval, Submarine	N_{SB}	4.0	Airborne, Unihabited, Attack	A_{UA}	6.0
Naval, Sheltered	N_S	4.0	Airborne, Unihabited, Fighter	A_{UF}	9.0
Naval, Unsheltered	N_U	5.7	Space, Flight	S_F	0.9
Naval, Hydrofoil	N_H	5.9	Missile, Free flight	M_{FF}	3.9
Naval, Undersea, Unshelled	N_{UU}	6.3	Missile, Flight, Airbreathing	M_{FA}	5.4
Airborne, Rotary, Winged	A_{RW}	8.5	Undersea, Launch	U_{SL}	11
Airborne, Inhabited, Cargo	A_{IC}	2.5	Missile, Launch	M_L	13
Airborne, Inhabited, Trainer	A_{IT}	3.5	Cannon, Launch	C_L	220
Airborne, Inhabited, Bomber	A_{IB}	5.0			

9.5 **Temperature Acceleration Factor**

Temperature acceleration factor, Π_T , is used to describe the effect of steady state temperature on component failure rates:

$$\prod_T = 0.1 \times \exp\left[-A\left(\frac{1}{T_j} - \frac{1}{298} \right) \right]$$

where T_j is the worst case junction temperature of the device, and A is a constant defined within the corresponding procedure. The constant depends on the device technology and on whether the component is in a hermetic or non-hermetic package. MIL-HDBK-217 identifies 25 types of IC technologies (e.g., TTL, LSTL, PMOS, NMOS, CMOS, HCMOS, etc.) which are grouped into 7 categories. It gives a value of A for hermetic and for non-hermetic components in each category.

T_j shall be measured or estimated using the following expression:

$$T_{jc} = T_c + R_{jc} \times P$$

where T_c is case temperature (^oC), P is the worst case power realized in a system application, and R_{jc} is junction to case thermal resistance for a device soldered into a printed circuit board. If the applied power is not available, use the maximum power dissipation from the device specification or from the specification for the closest equivalent device. If R_{jc} is not available, use a value contained in a specification for the closet equivalent device or use the following table.

Package Type	$R_{jc,max}$	Package Type	$R_{jc,max}$
14-lead FP(1/4"×1/4")	70	24-lead FP(3/8"×5/8")	53
14-lead FP(3/16"×1/4")	70	24-lead DIP(1/4"×5/4")	40
14-lead DIP(1/4"×3/4")	50	12-lead can	60
14-lead FP(1/4"×3/8")	70	8-lead DIP(1/4"×3/8")	50
16-lead DIP(1/4"×7/8")	50	40-lead DIP(9/16"×33/16")	30
16-lead FP(1/4"×3/8")	68	20-lead DIP(1/4"×17/16")	40
8-lead can	60	20-lead FP(1/4"×1/2")	60
10-lead FP(1/4"×1/4")	70	18-lead DIP(1/4"×15/16")	40
10-lead can	60	22-lead DIP(3/8"×9/8")	40
24-lead DIP(1/2"×5/4")	40	24-lead FP(1/4"×3/8")	55

For other devices, or if R_{jc} cannot be determined, use the following:

Package Type	Die Attach	Number of Package Pins ≤ 22 pins	Number of Package Pins > 22 pins
Hermetic DIPs	Eutectic	30	25
Hermetic DIPs	Epoxy or Glass	125	100
Nonhermetic DIPs	Eutectic	30	25
Nonhermetic DIPs	Epoxy or Glass	125	100
Hermetic Flatpacks	Eutectic	40	35
Hermetic Flatpacks	Epoxy or Glass	125	100
Hermetic Cans	Eutectic	30	NA

Hermetic Cans	Epoxy or Glass	125	NA

If the die attach method cannot be determined, assume that epoxy die attach is used for hermetically packaged CMOS and eutectic die attach for all other hermetic packages.

If T_C cannot be determined, use the following table.

Enviro.	G_B	G_{MS}	G_F	G_M	M_P	N_{SB}	N_S	N_U	N_H	N_{UU}	A_{RW}	A_{IC}	A_{IT}	A_{IB}
T_C	35	36	45	50	40	45	45	80	45	25	60	60	60	60
Enviro.	A_{IA}	A_{IF}	A_{UC}	A_{UT}	A_{UB}	A_{UA}	A_U	S_F	M_{FF}	M_{FA}	U_{SL}	M_L	C_L	
T_C	60	60	95	95	95	95	95	45	60	50	40	60	45	

9.6 Voltage Stress Factor

The voltage stress factor, Π_V, is 1 for all IC technologies except CMOS. For CMOS, Π_V is 1 for applied voltages of less t an 12 V. Above 12 V, Π_V increases exponentially with both the supply voltage and the device junction temperature:

$$\Pi_V = 0.11 \times e^{0.168 \times V_S (T_j / 298)}$$

9.7 Device or Process Learning Factor

Π_L reflects the fact that the first production units of any devices are more likely to be unreliable than later production units. Π_L is usually 1, but it is set to 10 under any of the following conditions:

1) A new device in initial production.
2) Major changes in design or process have occurred.
3) There has been an extended interruption in production or a radical change in line personnel.
4) For all new or unproved technologies.

9.8 Summary

Reliability predictions for microelectronic devices are especially important since they are key elements in improving reliability by increasing the level of component integration. This chapter introduces the reliability prediction procedure of MIL-HDBK-217.