Application Specific and Embedded DRAMs
(Applications, Trends and Technology)
May 2005

Dr. Betty Prince
Memory Strategies International
16900 Stockton Drive
Leander, Texas 78641
Phone: 512-260-8226
FAX: 512-260-3967
E-mail: bprince@memorystrategies.com
Past, current and future market numbers shown in this report should be considered as estimates. We make our estimates using numbers of units shipped because of our historical observation that units shipped tend to be more stable over time than revenues. Dollars shipped depend on the selling price of the units, a number which tends to be quite variable over time for electronic components. Our estimates of units shipped are revised from time to time to reflect the best market information we can obtain from open sources. There is, however, no guarantee of the accuracy of these sources. Future estimates are made to be continuous with our estimates of past trends. Many unforeseen factors can effect future predictions. These numbers should be used with great caution as the estimates that they are.
Table of Contents

1.0 Overview of eDRAM Chips Today
2.0 Embedded DRAM Applications and Market
  2.1 Networking
    2.1.1 Switches
    2.1.2 Network Processors
  2.2 Wireless
    2.2.1 Cell Phones
    2.2.2 Multimedia Cell Phones and Camera Phones
    2.2.3 Base-stations
  2.3 Computer
    2.3.1 L3 Cache in Servers
    2.3.2 Supercomputers
    2.3.3 Hard Disk Drive Controller
    2.3.4 Printer Engines
  2.4 Industrial Systems
    2.4.1 Industrial Communications:
    2.4.2 Industrial Processors
  2.5 Consumer Entertainment Systems
    2.5.1 Gaming Systems
    2.5.2 Televisions
    2.5.3 DVD Controllers
    2.5.4 Television Enabled PDA

3.0 Embedded DRAM Technology Today
  3.1 Overview
  3.2 Low Cost Adder eDRAM Cells
    3.2.1 Planar Capacitor Cells
    3.2.2 Two Shallow Trench eDRAM Cells
    3.2.3 MIM Capacitor Cells
    3.2.4 A One Transistor eDRAM on Bulk Silicon
  3.3 Mask Adders for various eDRAM Cell Types

4.0 Companies Supplying or Developing eDRAM or P-SRAM Products
  4.1 Agilent Semiconductor
  4.2 Chartered Semiconductor
  4.3 Dongbu Anam (DSP Foundry)
  4.4 Elpida
  4.5 Fujitsu
  4.6 Hynix
  4.7 IBM
4.8 Infineon
4.9 Kawasaki Steel
4.10 LSI Technology
4.11 Matsushita
4.12 Micron
4.13 NEC
4.14 Philips
4.15 Renesas:
4.16 Samsung
4.17 Sanyo
4.18 SMIC
4.19 Sony
4.20 ST Microelectronics
4.21 Toshiba
4.22 TSMC
4.23 UMC

5.0 eDRAM Cell Types by Supplier/Developer Company

Bibliography
1.0 Overview of eDRAM Chips Today

Chips with embedded DRAMs are being used today in a large number of applications. They are used in the consumer market in complex gaming consoles, for motion compensation in plasma screen television and DVD's, in multimedia cell phones and mobile phone base stations and in television enabled PDA’s. They are used in high end computer systems such as L3 cache in servers and in processors for supercomputers and also for computer peripherals such as printer engines and hard disk drive controllers.

Companies shipping chips with embedded DRAM are making them in an array of technologies. While this includes the conventional deep trench and stacked capacitor DRAM cells used in commodity DRAMs, it also includes DRAMs with planar capacitors, shallow trench capacitors, simple metal-insulator-metal (MIM) capacitors and those DRAMs with the capacitor integrated into the access transistor, the "capacitor-less DRAMs". Some of these embedded DRAM macros use SRAM-like interfaces and are marketed as SRAMs or P-SRAMs.

The criteria for optimizing a memory remains the same. Data storage must be low cost and adequate for the application. Lowering cost for an optimized DRAM relates directly to smaller chip size. For an embedded DRAM cost is also related to the increase in process complexity required to add it to a conventional logic process. Efforts to reduce process adders have led to the many variations in eDRAM cells.

Companies making embedded DRAM must first be making the logic that is integrated with the DRAM and have the structures set up to define and market the resulting logic chips or be supplying customers that have these infrastructures set up. Companies making eDRAM chips are therefore ASIC suppliers and pure play foundries whose customers require an easy to use high density RAM in the logic chip. It is IDM's making systems that can effectively use high performance chips with high density embedded memory such as those making gaming consoles or servers and super computers. It is also IDM's in various consumer markets such as high end television and computer peripherals. Some application specific DRAMs, that is DRAMs integrated with logic, such as standalone P-SRAMs are shipped by the commodity DRAM suppliers.

These issues are discussed in this report along with the companies making or developing chips with eDRAM.
2.0 Embedded DRAM Applications and Market

The concept of a "market" for a macro that is part of another circuit is difficult to discuss. It is, however, reasonable to talk about a market for a chip that contains eDRAM. These are the applications and market that will be considered here.

2.1 Networking eDRAM Applications

Switches and network processors were early high performance applications for embedded DRAMs since these applications require high density and high performance RAM.

2.1.1 Switches

In early 2005, Fujitsu was introducing leading edge Ethernet processing logic devices in 180 nm technology for volume production in March of 2005 with embedded SRAM. [12]

In October of 2003, NEC announced 130 nm silicon for a macro core and embedded DRAM for the System Packet Interface Level 4 Phase 2 (SPI-4.2). The macro was designed in NEC's CB-130 family which runs in .95 nm technology. The eDRAM runs at 200 MHz random access and was said to provide higher density, higher speed, lower power and lower SER for high end communications applications. SPI-4 is used for exchanging packets between physical layer (PHY) devices and the rest of the 10 Gbps SONET/SDH system, such as OC-192/STM-64 SONET/SDH routers and Packet over SONET (POS) applications. SPI-4.2 is the latest version of the SPI-4 standard and specifies a higher-speed and narrower interface than the first version. SPI-4.2 calls for separate transmit and receive interfaces, delivering faster performance by allowing for the simultaneous exchange of data packets.[77]

TSMC runs in production a 250 nm networking chip with 4Mb of eDRAM in the MoSys 1T-SRAM cell type. This part runs with 81% yield. They also run a 220 nm 2-Mb eDRAM networking chip with the same cell with 86% yield. [132]

2.1.2 Network Processors

In February of 2005, Matsushita discussed target applications of 150 nm logic based shallow trench eDRAMs as being network processors using multiprocessing for real time multimedia and broadband networking applications. A Network processor with 13.5 Mb of eDRAM was shown. A 400 MHz 1.5V dual ported interleaved eDRAM was developed in a 150 nm CMOS logic process with 10 fF capacitance in a shallow trench technology.[61]
In April of 2003, EZChip announced their NP-1C Network Processor, made at IBM, which runs at 62 Gbytes/s of memory bandwidth on a 2048 bit bus with 8 banks of eDRAM. The bandwidth is to enable multiple table lookups per packet at 10 Gbits/s. The 4-Mbytes of embedded DRAM adds about 30 mm2 to the die size.[64]

2.2 Wireless eDRAM Applications

2.2.1 Cell Phones with P-SRAM

Cell phones use RAM as main memory along with flash memory for data and code storage. Because of the small form factor requirements, these standalone memories are frequently packaged in multichip modules. The RAM used tends to be 6T cell SRAM in low end phones requiring less than 2MB of RAM and to be P-SRAMs (eDRAMs with an SRAM interface) in cell phones such as multifunction phones which require more working memory.

An estimate of the market for units of cell phone shipments is shown in the following chart. If we assume that one P-SRAM is shipped in each cell phone and that 60% of the RAMs in cell phones in 2004 were P-SRAMs and a reasonable conversion rate to P-SRAM over time, then an estimate of the number of P-SRAMs shipped in cell phones over time is also shown in the following chart.

Estimate of P-SRAMs Shipped in Cell Phones by Year.
Some companies making P-SRAMs are noted below.

In March of 2005, Elpida introduced their 512 Mb and 256 Mb DDR and SDR x32 and x16 Mobile RAMs in 100 nm technology to production as bare chips for stacking in multichip packages for video and multimedia cell phone applications. Data transfer rate is 333 Mbps at 1.8 V. These parts have identical bonding pad order between densities to simplify stacking. The interface supports single edge and double edge layout.[63]

Fujitsu makes Fast Cycle RAMs which are DRAMs with an SRAM interface (PSRAMs). They make these from 16-Mb density to 128 Mb density. In November of 2004, Fujitsu announced sampling of their 128-Mb Mobile FCRAM which complies with the COSMORAM spec for mobile phone applications. This part is a PSRAM (DRAM). It has burst operation at 108 MHz with 1.8 V supply. Standby current is 300 uA with lower current (10 uA) in sleep mode and partial array power down. It has a 32-bit address/data muxed bus to reduce the pin count. Access time (Tac) is 6 ns and access from clock is 70 ns. The COSMORAM spec is a common specification of Fujitsu, NEC and Toshiba.[16] [17]

In November of 2004, NEC introduced a 128 Mb P-SRAM (DRAM) standardized to the COSMORAM Rev. 3 specification for low power operation. Toshiba and Fujitsu cooperated with NEC in the development of this standard for the advanced mobile handset market. The μPD46128953 runs at 83 MHz in burst mode at a voltage of 1.8 V. Integrated onto the chip is a delay circuit for regulating the internal pulse mechanism, a 32-bit interface, and three driver output settings to adjust for noise level. The parts were available in December of 2004 and expected to be in mass production starting in March of 2005. Monthly production volumes are expected to reach 1 million units per month. [78]

In June of 2004, Infineon announced a 16-Mbit and 32-Mbit CellularRAM for the wireless handset market. These parts operate at 1.8 V with 70 nm SRAM access time and 80 MHz burst frequency. Samples of the 64 Mbit were expected in 4Q04 and 128 Mbit is planned for 1Q05. These PSRAMs are for use in 2.5G and 3G handsets with multimedia and camera features. Infineon and Micron offer CellularRAM at 1.8 V.[54]

Hynix’s 150 nm technology is being used to run standalone DRAMs. They currently offer a 2 Mx16 P-SRAM. It is targeted at the mobile phone market.[18]

Micron makes the Cellular RAM which is a DRAM with an SRAM interface for the mobile handheld system markets. In July of 2004, Micron Technology started producing 128-Mbit PSRAMs of the CellularRAM type. They indicated that in mid 2004 PSRAMs have overtaken 6T SRAMs in cell phones with a peak of 60% of the RAM market for cell phones.[62]
STM makes a line of PSRAMs which are delivered in modules with flash memory for use in mobile terminals. These include 16Mb, 32Mb and 64Mb PSRAMs. These parts are made in 130 nm, 150 nm and 180 nm technologies. Target applications for these PSRAMs are wireless and portable communication products which have higher density requirements than can be provided cost effectively by 6T SRAMs along with low power storage requirements. Specific applications mentioned are portable Java machines and systems with streaming functions such as 3G mobile phones.[116][117]

Toshiba offers P-SRAM from 32-Mb to 128-Mb densities that are widely used in cell phone applications. Toshiba's P-SRAM has DRAM array and an asynchronous SRAM external interface. It is based on the COSMORAM specification defined by Toshiba, NEC, and Fujitsu. Toshiba intends to support up to 256Mb density during 2005. [125]

TSMC has in production a 180 nm 10-Mbit eDRAM chip using the 1T-SRAM cell for handheld systems. The part has 80% yield [132]

### 2.2.2 Multimedia Cell Phones and Camera Phones

High end multimedia cell phones such as camera phones also tend to use a multimedia chip which is some cases has an embedded DRAM.

In February of 2005, Renesas and Matsushita discussed target applications of the next generation of the logic-based MIM eDRAM in 90 nm technology as being multimedia driven digital consumer electronics specifically multimedia mobile applications such as high end cell phones, PDA's, etc. [91]

NVidia's GeForce 2100 is an older rebranded MediaQ processor and their newest part is the GeForce 2150 which is also a chip design done by MediaQ before the acquisition. It is targeted to appear in cell phones. The 2150 adds acceleration for digital camera phones with resolutions up to 1.3 megapixels. It includes 160 KB of eDRAM with a 64-bit wide interface. This is enough for a 320 x 240 display to be refreshed entirely within the chip which reduces power consumption. The chip has less than 10mW power during JPAG encode. The fast encode allows the display to update more quickly which reduces jerky motion when lining up a shot. New products using the GeForce 2150 were expected to appear in the first half of 2004. NVidia's follow-on chip is expected to add 3D capability for cell phones and PDA's. [45]

In February of 2004, Renesas discussed the target applications of a logic-based eDRAM in 130 nm technology as being the high end cell phone and PDA market where devices require large embedded memory arrays for multimedia processing and also require low power and high performance. [89]
2.2.3 Basestations

The TigerSHARC ADSP-TS201, ADSP-TS202 & ADSP-TS203 family with eDRAM, announced by Analog Devices in June of 2003, was claimed to do signal processing at lower cost and power consumption than with SRAM-based solutions. The eDRAM leakage per bit for the IBM eDRAM was claimed to be less than 1/100 that of SRAM and system level reliability was claimed to be higher due to low susceptibility to memory SEU with the SER of eDRAM claimed to be more than 1000 timers better per bit than SRAM. Target applications were: next generation base stations, 3-D imaging systems, and radar and sonar applications.[40][41][42]

Also in June of 2003 ADI indicated the target market for the TigerSharc line includes the wireless infrastructure, for baseband IC for wireless basestation, a market which is estimated at nearly $750 million in 2003. The TigerSharc can be used to implement a software defined radio where instructions are written into the DSP eliminating the need for a second supporting ASIC. ADI indicated that they were getting a significant number of design wins in this area and expected to move to a leadership position against their main competitors who are TI and Motorola. At the time ADI had no significant market share in this area.[41]
2.3 Computer

Embedded DRAM has been discussed for high density and high performance computer applications such as L3 cache in servers and in main memory in supercomputers. It has also been targeted in peripheral computer applications such as hard disk drive controllers and printer engines.

2.3.1 L3 Cache in Servers

In February of 2004, IBM discussed a 500 MHz eDRAM macro made in 90 nm technology which was targeted at competing with 2ns eSRAM speeds in the same technology. The macro was compilable, used multi-bank interleaving and used a direct write method for restore. The random bank cycle time was reduced 33% over the previous design. The 500 MHz data rate used a configurable 4-stage pipeline which reduced the cycle time to 2ns. Trench eDRAM cell size is 0.1848um2. The local arrays are organized 512 rows by 8 columns by 128 or 146 bits and contain local row drives, sense amps and control logic. The largest macro is 73 Mb with 33.72mm2 area. An embedded DLL controls the read pipeline and write back timing. BIST is included.[21]

The DRAM cycle is segmented and direct write is used in which data is placed on the bitline before the wordline is activated. To prevent preamplification of the bitlines a PFET set device is used. For the pipeline operation a precharged predecoded address bus is used and addresses are predecoded during clock buffering. Local refresh address counters in each bank improve user control of bank address during refresh. The piped data is routed to a set of read steering switches which time aligns it.[21]

In February of 2003, IBM indicated that some of their servers, such as the X series had L3 cache that is eDRAM and their eDRAM Group Leader indicated that he expected that all L3 cache would be eDRAM in the future. At the same time he indicated that it was unlikely that the trade-offs would put eDRAM in L2 cache. [23]

2.3.2 Supercomputers

DARPA Petaflops Computer:
In July of 2003, IBM proposed an eDRAM cache technology in the 3 year R&D DARPA petaflops computer competition with Cray and Sun. The DARPA criteria are 10-40 times the performance of current high performance machines and also easier to program. IBM proposed building a PowerPC processor-based system with up to a gigabyte of eDRAM cache. The processor is intended to be a complete subsystem.[33]
BlueGene:
In 2004 the BlueGene/L Motivation processor is designed in IBM's 8SF technology which is 130 nm copper. It uses two 700 MHz PowerPC 440 processors, a SIMD like floating point instruction extension and 4MB of eDRAM as shared L3 cache. [35][36]

The IBM Blue Gene supercomputer was developed as a research project in 2000 but is now a commercial product sold by the IBM server group under the name eServer Blue Gene. It sells for $1.5 million and up. It is sold in configurations of 1 - 64 racks. Each rack has 1024 processors. A 16-rack configuration holds the world’s performance record at 70.7 trillion calculations per second (teraflops). Customers include: The San Diego Supercomputing Center who plans to install a one rack system in December of 2004 for cosmological research. In October of 2004, IBM moved a system to the Lawrence Livermore Labs. Other Blue Gene customers include: Japan’s National Institute of Advanced Industrial Science and Technology, the Lofar radio telescope run by Astron in the Netherlands, and Argonne National Laboratory. IBM launched the Blue Gene project in 2000 as part of an effort to speed calculations that predict how strings of biochemical building blocks, encoded by DNA, fold into large molecules called proteins. [37]

The Blue Gene Server runs on sub-GHz processors with numerous low frequency cores on a single piece of silicon with lots of embedded memory. By using slower chips IBM keeps the power and heat low permitting a system that fits into a small space. [207] The Blue Gene Server uses a PowerPC 440 700 MHz processor with two processors per chip. External memory is 512 MB of DDR SDRAM per node.[38]

2.3.3 Hard Disk Drive Controller

Embedded DRAM has been used in hard disk drive controllers due to formfactor constraints which dictate a one chip solution for a controller that also requires a high bandwidth, wide bus memory.

The Super10 Nova Hard Disk Drive controller is made in STM's advanced 130 nm technology. They have a specific version of the HSMOS9 process made with features for hard disk drives with eDRAM and eDRAM capability along with a high speed Super10 MCU and analog circuitry. The Nova Disk Manager chip includes a disk controller, 150 MHz Super10 DSP and eDRAM intended to increase the memory access bandwidth. The 16-bit wide e-DRAM interface is capable of 225 MB/s bursts permitting sustained data transfers between the DMA interface and the read channel with concurrent accesses for DRAM refresh, ECC, servo table management, cache table access, detect list searches and general DSP access. The "enhanced Super10" provides a set of features specially tailored for the hard Disk Drive Market. External power supply is 3.3V and internal power supply is 1.8 V. [111][112]
2.3.4 Printer Engines

Printer engine chips tend to use embedded DRAM due to the density of RAM required in the chip. Ink jet printer engines in 2004 use between 8-Mbit and 32-Mbits of wide bus RAM. This is too much RAM to make cost effectively with SRAM so DRAM tends to be used. It is efficient to integrate the DRAM on the chip since such small densities of DRAM are not generally available and the integration of wide bus RAM on chip reduces the print engine formfactor and cost.

In April of 2003, STM started production of a Digital Printer Engine with embedded DRAM in 180 nm technology. They also announced a new digital printer engine SoC taped out in 130 nm technology. They had previously announced contracts with two leading printer manufacturers to develop system-on-chip solutions with embedded DRAM memory for the digital printer engines' used in inkjet printers. [110]

An estimate of shipments of hard disk drive controller and printer engines shipped by year is shown in the following figure. It is not clear what percentage of these markets use chips with eDRAM.

Estimated Shipments of Computer Peripherals (mu)
2.4 Industrial Systems

2.4.1 Industrial Communications:

In June of 2004, Infineon published the 2.4 version of their TC11IB datasheet with 12 Mb of eDRAM. Infineon discussed their TC11IB TriCore MCU 32-bit MCU, in January of 2002. The part has 1.5 MB (12 Mb) of eDRAM on chip along with PCI and Ethernet interfaces. It was made in the 180 nm process. The MCU is targeted at industrial communications devices. The eDRAM is intended to provide sufficient memory in a single chip for sophisticated real-time operating system use. Applications include: Programmable Logic Control (PLC), Industrial bus controllers, Motion control, Human/Machine Interfaces (HMI), PC-based applications, Gateway PCI - Ethernet and General purpose industrial devices. The latest revision of the datasheet for this part was in February of 2002.[52][53]
2.5 Consumer Entertainment Systems

Consumer entertainment systems such as game consoles, televisions and DVD players tend to have multimedia requirements which dictate high performance and large memories. They are frequently also portable requiring low power and small formfactor. These are all criteria which tend toward use of processors with embedded DRAM.

2.5.1 Gaming Systems

Several of the gaming systems on the market and in development today use embedded DRAM and are discussed in this section. These systems require high density memory with high performance interfaces. This can be obtained by integrating the memory on the chip and still maintain the low power required in portable systems. The chart below indicates an estimate of the size of the gaming system market over time. It is possible that as much as half of this market is served by systems with multimedia processor chips using embedded DRAM.

**Estimate of Gaming Consoles Shipped over Time (mu)**

![Estimates Game Console Shipments (mu)](image)

**Xbox2:**
Microsoft's Xbox2 console will use three IBM PowerPC G5 class 64-bit processors which will be fabbed in 65 nm technology at IBM. It was not reported whether these processors would use eDRAM or not. [46]
In April of 2005, NEC announced that Microsoft has adopted the NEC eDRAM technology for the next generation XBox game console. Production of the eDRAM graphics chip is underway at NEC's 300 mm wafer fab in 90 nm UX6 technology. [80]

The ATI 360 GPU for the Microsoft XBox is a two chip system on a single substrate in a single package. One chip has the GPU and memory controller and the other chip has a 10 MB center of eDRAM designed by NEC surrounded by a ring of logic designed by ATI. The two chips are connected by a 256 GB/sec bus interface. The logic on the eDRAM chip is 192 basic math processors for multisampled antialiasing. The processors handle 32 pixels at one time by operating on six components per pixel: red, green, blue, alpha, stencil and depth. This gives the XBox 360 4X antialiasing ability on a 1280c768 image with negligible performance penalty. The eDRAM architecture contributes to a low power design. [143]

**Nintendo:**

NEC also makes the ATI/Nintendo "Flipper" chip which is manufactured in NEC's 180 nm embedded DRAM process. The clock frequency is 162 MHz. It has 2 MB of embedded frame buffer made with the 1T-SRAM (embedded DRAM) with sustainable latency of 6.2 ns. It has 1-MB of embedded texture cache with 6.2 ns latency made of 1T-SRAM. The peak texture read bandwidth is 10.4 GB/second. The main memory peak bandwidths is 2.6 GB/s and Pixel Depth is 24-bit color with 24-bit Z buffer. Image processing functions include: fog, antialiasing, alpha blending, virtual texture, multi texture, bump mapping, environment mapping, MIP mapping, bilinear/trilinear/anisotropic filtering, decompression and deflickering. [67]

NEC has a 180 nm technology eDRAM Chip in Nintendo's GameCube. NEC shipped more than 4.5 million units by March 2002 after an aggressive ramp-up to meet the gaming system schedule. The chip has two large blocks of eDRAM. One is 16-Mbits and the other is 8-Mb. Random access time is 6.17 ns. The DRAM cell is the MoSys 1T SRAM macro. [74]

**Sony Playstation2**

The Sony Playstation2 uses 2-Mbytes of eDRAM. [103]

**Sony PSP:**

The Portable Sony Playstation (PSP) was introduced in March of 2004 with 8-Mbytes of main memory embedded in the MIPS 4000 processor core, 2-Mbytes of memory embedded in the media engine and 2-Mbytes of eDRAM in the graphics core. The Sony PSP was scheduled to go on sale late in 2004 in Japan and during 1Q05 in North America. Sony has indicated that it plans to ship 3 million units of the PSP by March 31, 2005. [103]
**Hudson Soft:**
In March of 2005, MoSys announced that Hudson Soft, a manufacturer of game software and entertainment equipment had successfully verified MoSys 1T-SRAM technology, which uses a planar eDRAM cell, in UMC's 150 nm process. The Hudson Soft Video Game Controller has a 32-bit network CPU and is used in electronic toys made in Japan. [136]

### 2.5.2 Televisions

Chips with eDRAM have been used in high end TV sets for motion compensation and scan conversion as well as for special features such as picture-in-picture (PIP) for many years.

In July 2003, Philips introduced their SAA4998 high end motion compensation/estimation chip for 100 Hz and progressive scan LCD or Plasma TV. This chip, which uses 9-Mbits of 180 nm technology embedded DRAM, addresses format conversion and enhancement for the various frequency rates and display formats of modern television. Philips makes the chip at their Crolles 1 wafer fab in France. The chip reduces blur and judder during fast motion sequences in film, TV and DVD. Edge dependent de-interlacing results in sharper characters and diagonal lines and motion compensated picture interpolation reduces blur. Blur is a pitfall in LCD panels. For DVD the motion compensation reduces judder. The chip does 100 Hz conversion and permits 60 Hz LCD panel use in 50 Hz regions (Europe, Asia) with judder free 50Hz to 60 Hz conversion. It does conversion from the 24/25/30 Hz used in film and the 50/60 Hz used in video input material. It handles both interlaced and progressive scan output formats ranging from 50 to 120 Hz. It can output to DLP screens. New algorithms include: a 3-D recursive search motion estimator and a new deinterlacing algorithm. The motion estimation and conversion algorithms from the earlier chips are used. A cost optimized version, the SAA4999A, was also introduced which uses embedded DRAM. [83] [94]

On 100 Hz LCD screens the SAA4998 reduces blur and permits 60 Hz LCD panels to be used in 50 Hz regions. Video is enhanced on 100 Hz Plasma displays where the motion compensation reduces judder. For movies the film is recorded at 24/25/30 Hz. The sub-pixel accuracy of the motion estimator models camera caused motion well. Motion conversion is adapted to all video and film input picture rates. It automatically recognizes the original picture rate on input video. The SAA4998 family was sampling in July 2003 and in volume production in August of 2003. [83]

Loewe Opta, a high end TV manufacturer, indicated that they used the SAA4998 chips in their TV's which are based on matrix displays using: PDP(plasma display panels), LCD (liquid crystal displays), and DLP(Digital Light Processing - TI's digital micro-mirror-devices). They were the first company to apply this technology for the consumer market in their Spheros-42-HD launched in July of 2003. [83]
In May of 2003, Loewe announced their Spheros 42 HD 42” plasma screen TV with 1024 x 1024 pixel resolution which uses the Philips SAA4999A motion compensation technology. Various multimedia features can be added such as encrypted satellite, digital pay TV, etc. can be added and used with an activated smart card. The set is also web enabled and can add home automation control features.[83]

2.5.3 DVD Controllers

In May of 2003, MoSys announced that LSI Logic was making IC's for DVD applications using the MoSys 1T-SRAM eDRAM technology.[59]

Philips makes a module, the MK14-EM Module, which helps implement their SAA4998 motion compensation and scan conversion eDRAM chip. For DVD the SAA4998 eDRAM chip reduces blur and judder during fast motion sequences in film, TV and DVD. For implementing motion compensation in a DVD Player which usually contains movie material conversion is required from 24 pictures/second and TV artifacts must be removed. The module requires one SAA4998 using eDRAM as shared field memories and one SAA4979 using one eDRAM as embedded field memory. For implementing Picture-in-Picture (PIP) in TV Applications the module requires two SAA4998 and one SAA4979 since PIP must be implemented with one of the SAA4998.[96]

An estimate of shipments of high end DVD Recorder/Players is shown in the following chart.

**Estimated Shipments of High End DVD Recorder/Players (mu)**

![Estimated Shipments of DVD Recorder/Players (mu)](image)
2.5.4 Television Enabled PDA

In January of 2005, Sony described a microprocessor made in 180 nm CMOS eDRAM technology for high performance audio and video in multipurpose handheld PDA applications with 128-bit wideband 64-Mb eDRAM. The processor used a dynamic voltage and frequency management scheme with leakage power compensation. Movie applications were targeted. Power consumption targeted for these applications is typically 250 mW including 75 mW for audio, 50 mW for scheduling and 3 mW for standby. The processor has four 128-bit data width 16-Mb eDRAM macros. Processor blocks are connected to the eDRAM by a 128-bit bus. A 2-D graphics engine is included on the chip. The maximum data transfer rate of the wideband bus is 7.86 GB/s. [142]
3.0 Embedded DRAM Technology Today

3.1 Overview

There are many companies shipping logic chips with embedded DRAM. The motivation of these suppliers with regard to DRAMs is primarily to provide high density RAM memory that is adequate for the application at the lowest possible cost. DRAM is here defined as a memory chip with a cell consisting of one access transistor and one storage capacitor. There is a large assortment of technologies used for embedded DRAMs.

Those who use embedded DRAM have the same motivation as those making commodity standalone DRAM which is to make a high density RAM at a low cost. Standalone DRAM chips accomplish this cost reduction by using capacitors that are optimized for small lateral chip area in order to minimize the size of the chip and increase the number of chips per wafer thereby reducing the cost of the individual chip. Embedded DRAMs can be most effectively reduced in cost by making the capacitor formation process as close to the logic process as possible even if the area of the memory array is increased slightly.

The cost of an embedded DRAM depends on how many critical processing steps, i.e. masking steps, must be added to the standard logic process to add the DRAM array to the chip. The embedded DRAM macro also needs to have a cost or performance advantage over macros of competing technologies primarily SRAMs. The cost advantage is usually a smaller cell size permitting higher density on the chip. The performance advantage tends to be lower power or lower soft error rate. Embedded DRAMs intended for use with high performance logic must have a low thermal budget requirement for the process after the logic transistors are formed.

Historically there were two types of high density embedded DRAM: Stacked and Trench. Today embedded DRAM technologies range from simple planar DRAM cells to a large assortment of trench and stacked capacitor cells.

Embedded DRAM technologies that gain lateral area by trenching down into the silicon include: shallow trenches, deep optimized trenches. Trench eDRAMs have planar transistors and in scaled processes can have vertical transistors.

The trench eDRAM is an optimized DRAM with a small cell size. For high density eDRAM used in high performance systems such as gaming systems, a trench DRAM provides a high density array without affecting the performance of the logic transistors since the high temperature process for forming the trench capacitors takes place before the logic transistors are formed. The trench capacitor process, however, takes 4+ additional masking steps which makes it a high cost process if high density eDRAM and high performance are not required.
Embedded DRAM technologies that gain lateral area by stacking above the silicon include: silicon-insulator-silicon (SIS) stacks, metal-insulator-metal (MIS) stacks, and capacitors in the interconnect structure such as metal-insulator-metal (MIM) stacks.

Materials for capacitor insulator include the conventional SiO2 and SiON and higher dielectric constant materials such as Ta2O5, Al2O3, HfO/Al2O3 laminate and others.

Some newer candidate cells for embedded DRAM have no capacitors, the so-called capacitorless DRAMs. Many of the capacitor-less DRAMs are made on SOI substrates.

3.2 Lower Cost Adder eDRAM Cells

3.2.1 Planar Capacitors for eDRAM

Some embedded DRAMS, such as those with planar capacitors, do not add any process steps to the conventional CMOS logic process. A planar capacitor embedded DRAM macro packaged with an interface can be used in the logic process like any other macro. An example is the macro from MoSys Inc., called a 1T-SRAM, which packages a planar DRAM cell array with an SRAM interface and various house-keeping features such as error-correction. An illustration of a planar capacitor cell showing the capacitor and the access transistor is shown below.

The advantage of the planar capacitor eDRAM is no cost adder to the CMOS process. This is traded-off with a larger cell size and a lower capacitance than a more optimized eDRAM process.
3.2.2 Shallow Trench Capacitors for eDRAM

Between the planar capacitors that add no process cost and the optimized stacked and deep trench capacitors, there is a range of capacitors used in embedded DRAMs.

The Shallow Trench Capacitors, which are simple planar type capacitors with the capacitor dropped into a shallow trench, increase capacitor area over the planar capacitor without increasing lateral area while adding only one masking step.

The MoSys "1T-SRAM-Q" cell, which some foundries use at the 130 nm node, and the Matsushita "Striped Trench" cell fall into the shallow trench category.

MoSys 1T-SRAM-Q Cell:

A concept schematic cross-section of the trench "Q" cell developed by MoSys is shown below.

Schematic Cross-Section of Shallow Trench Capacitor eDRAM Cell[132]
(MoSys "1T-SRAM-Q")

Area is added to the capacitor plate by the additional vertical area above the gate oxide which is trenched down into the trench isolation.

Matsushita Striped Trench Cell:
Another method of making a simple one mask adder shallow trench cell is the Matsushita striped trench cell.
A concept schematic cross-section of this cell is shown in the following figure.

**Schematic Cross-Section of Shallow Trench Capacitor eDRAM Cell[61]**
(Matsushita "Striped Trench" cell)

![Schematic Cross-Section of Shallow Trench Capacitor eDRAM Cell](image)

### 3.2.3 MIM Capacitor eDRAM Cells

A new type of DRAM cell, now being widely adopted for embedded DRAMs at the 90 nm technology node and beyond, uses a stacked metal-insulator-metal (MIM) capacitor which is formed in the interconnect structure of the logic chip and adds only one or two masking steps to the logic process. The capacitance of the MIM capacitor can be increased by using a higher dielectric constant material than SiO$_2$ for the capacitor dielectric. Ta$_2$O$_5$ or SiON, for example, are used if they are already available in the process. The MIM capacitor is being used by eDRAM foundries such as TSMC and NEC at the 90 nm node and below. A MIM capacitor eDRAM cell concept is illustrated below.

**Schematic Cross-Section of a MIM Capacitor eDRAM Cell**

![Schematic Cross-Section of a MIM Capacitor eDRAM Cell](image)
3.2.4 A One Transistor eDRAM on Bulk Silicon

Embedded DRAMs made from a single transistor with no external capacitor are still in development. A low cost one with one additional non-critical mask and three process steps added to conventional 130 nm CMOS logic was shown by ST Microelectronics in June of 2004. This one transistor cell is constructed on a triple well structure NMOS FET. [115] A schematic cross-section of this cell is shown in the following diagram.

STM Capacitorless DRAM on Bulk NMOSFET[115]

3.3 Mask Adders for Various eDRAM Cells

The number of masking steps which various companies have indicated are added for these DRAM capacitor types are shown in the following table.

Mask Adders to Standard Logic for Various DRAM Capacitors

<table>
<thead>
<tr>
<th>Capacitor Type</th>
<th>Masks Added</th>
</tr>
</thead>
<tbody>
<tr>
<td>Planar Capacitor</td>
<td>0</td>
</tr>
<tr>
<td>Deep Trench</td>
<td>3-8</td>
</tr>
<tr>
<td>Shallow Trench</td>
<td>1</td>
</tr>
<tr>
<td>Optimized Stack</td>
<td>4-8</td>
</tr>
<tr>
<td>MIM Stack</td>
<td>1-2</td>
</tr>
<tr>
<td>One Transistor</td>
<td>1</td>
</tr>
</tbody>
</table>

The planar capacitor, shallow trench and MIM stack are clearly lower cost eDRAM processes than either the deep trench or optimized stack processes. The deep trench or optimized stack, however, can be a higher density process. The deep trench can offer higher performance.
4.0 Companies Developing or Supplying Chips with eDRAM or P-SRAM

4.1 Agilent Semiconductor

In January of 2004, MoSys announced that Agilent had licensed the 1T-SRAM-R embedded memory technology for use in the Agilent ASIC and SoC products. [2].

In August of 2004, Agilent announced validation of its Chip Wrights DSP core in an SoC made in 90 nm ASIC technology. Agilent supplies chips for desktop printer and imaging ASIC applications potentially for their own system divisions. [3]

Agilent has a wafer fab in Fort Collins, CO, and participates in a foundry venture in Singapore.

4.2 Chartered Semiconductor

Chartered is a Pure Play Foundry. They have announced use of the MoSys type 1T-SRAM in their logic foundry chips with high density RAM requirements.

In January of 2005, IBM and Chartered announced an extension of their joint development agreement to include 45 nm bulk CMOS technology in addition to the 90 nm and 65 nm already agreed on. The two companies are developing processes for 300 mm wafers. The agreement was extended though June of 2008. Separately at a presentation made by the two companies in July of 2004, they indicated that IBM's embedded DRAM trench technology was not included as part of the joint agreement.[5]

In July of 2004, Chartered and MoSys announced validation of the MoSys 1T-SRAM-Q silicon in Chartered's 130 nm logic process. Full qualification is expected by 4Q2004. The 1T-SRAM-Q uses MoSys' folded capacitor which folds the bit cell gate oxide capacitor vertically down the STI sidewall increasing capacitance without increasing lateral area on the chip. Bit cell size is 0.57 um2 in 130 nm CMOS technology and macro density is about 1.2 mm2/megabit. The macro also has error correction to either eliminate laser repair or improve soft errors. The planar 1T-SRAM-R technology of MoSys was already qualified by July of 2004 on Chartered's 180 nm and 130 nm process. Both companies indicated they plan to qualify the technology on the 90 nm process. [4]

Chartered operates 5 fabs in Singapore with the capability of producing 1.5 million 8" equivalent wafers per year by 2003. Their sixth fab, a 300 mm facility entered pilot production in 3Q04 and was expected to bring on-line an additional capacity of 30,000 12" wafers (67,500 8" equivalents) per month.[4][7]

4.3 Dongbu Anam (DSP Foundry)

In September of 2004, Dongbu Anam was the fourth largest pure play foundry. In that month they announced the silicon verification of the MoSys 1T-SRAM technology on their 180 nm technology and had begun verification of the 1T-SRAM on 130 nm CMOS technology. [9] Dongbu Anam's web page in April of 2005 shows the 1T-SRAM available in both their 180 nm and 130 nm CMOS technology. [10]

Dongbu started out in 2001 with a 5,000 wpm line which ran 250 nm technology licensed from Toshiba. 180 nm technology was qualified in 2002 and 130 nm was in development. In 2002, Toshiba gave Dongbu access to the Toshiba cell library of analog, logic and I/O functions and a contract with Toshiba to supply parts.[12] The MoSys eDRAM technology can be used with the cell library to make ASIC and logic products.

Dongbu in 2002 acquired a controlling 33% interest in Anam and by the end of 2003, Dongbu-Anam was merged into a single functioning entity. In 2002, they lost a $400 million contract to make parts for Texas Instruments which would have allowed them to move to 130 nm technology.[11] By 2003, Dongbu Anam was making 10,000 wafers per month of DSP chips for Texas Instruments, but this was expected to decrease as TI moved its DSP to 130 nm since Dongbu Anam did not at the time have 130 nm technology.[8]

4.4 Elpida

While Elpida doesn't appear to do embedded DRAM in logic, they do make PSRAMs which are DRAMs embedded in an SRAM interface and Mobile RAMs for portable applications.

In March of 2005, Elpida introduced their 512 Mb and 256Mb DDR and SDR x32 and x16 Mobile RAMs in 100 nm technology to production as bare chips for stacking in multichip packages for video and multimedia cell phone applications. Data transfer rate is 333 Mbps at 1.8V. These parts have identical bonding pad order between densities to simplify stacking. The interface supports single edge and double edge layout. Production is expected to begin in 2Q05. Elpida offers DRAM based products for servers, mobile phones, digital TV, digital cameras and PC's. Elpida's sales for fiscal year 2004 were Y100.4 billion.[13]
Elpida is a joint venture of NEC's and Hitachi's former DRAM businesses formed in 1999. In October of 2002, Mitsubishi's DRAM business was also added to the venture including their devices and IP produced on 150 nm process and smaller. Powerchip Semiconductor, who had been a foundry for Mitsubishi was to become a foundry for Elpida using the 130 nm process acquired from Mitsubishi. They will then move to a 110 nm process being developed by Elpida. Mitsubishi would continue to use Powerchip for their System LSI products including those with embedded DRAM. Elpida's research, design and development operations were merged from NEC and Hitachi on April 1, 2000 and sales and marketing operations commenced in Q1, 2001. [14]

Elpida indicated in March of 2005 that they were seeing a very low ramp of DRAMs in SMIC's Beijing operation and was focusing on their relationship with Powerchip which had a 300 mm fab in production and was due to start production in a second 300-mm wafer facility in the third quarter of 2005.[15]

4.5 Fujitsu

Fujitsu makes logic chips with eDRAM and provides eDRAM foundry service. They also make PSRAMs for the mobile phone market.

In April of 2005, Fujitsu announced that they would use the MoSys 1T-SRAM-Q bit cell technology in their 90 nm ASIC and SoC designs for portable consumer applications and also in their ASIC foundry services. The Q-cell is trenched down into the STI to provide additional capacitive surface area. [17]

In January of 2004, Fujitsu indicated that they would use the MoSys 1T SRAM for embedded DRAM technology in their 130 nm logic process rather than conventional optimized embedded DRAM technology. The reason given was the simpler and more logic compatible embedded DRAM process provided by MoSys in addition to the design simplification of using the SRAM interface on the embedded DRAM. The 1T SRAM uses a simplified DRAM cell with on-chip refresh which is transparent to the users. The planar capacitor is made in standard CMOS with no mask adders. [16]

In early 2005, Fujitsu was introducing leading edge Ethernet processing logic devices in 180 nm technology for volume production in March of 2005 with embedded SRAM [12] and also introducing 32-bit RISC Flash microcontroller chips in 350 nm technology for industrial applications with embedded SRAM. [13]

Fujitsu also makes 16-Mb - 128-Mb Fast Cycle RAMs which are DRAMs with an SRAM interface (PSRAMs). In November of 2004, Fujitsu announced sampling of their 128-Mb Mobile FCRAM which complies with the COSMORAM spec for mobile phone applications.
This P-SRAM has burst operation at 108 MHz with 1.8 V supply. Standby current is 300 uA with lower current (10 uA) in sleep mode and partial array power down. It has a 32-bit address/data muxed bus to reduce the pin count. Access time (Tac) is 6 ns and access from clock is 70 ns. The COSMORAM spec is a common specification of Fujitsu, NEC and Toshiba.[16] [17]

4.6 Hynix

Hynix's 150 nm technology is being used to run standalone DRAMs. They currently offer a 2Mx16 P-SRAM. It is targeted at the mobile phone market.[18]

4.7 IBM

Overview of IBM's Venture Development Partners:
IBM and their DRAM venture development partners originated the optimized trench capacitor cell DRAM. IBM participated in the commodity DRAM market until July of 1999 when they sold their share of the joint IBM/Toshiba DRAM Dominion Semiconductor Fab to Toshiba. This was effectively the end of IBM's production of commodity DRAMs. They announced at the time that their DRAM efforts at that point were going to go into eDRAM in ASICs.[19]

In March of 2004, Samsung announced that it was joining the technology development partnership with IBM, Chartered and Infineon to develop 65 nm technology and extend over time to 45 nm technology. A separate agreement with IBM gave Samsung license rights to IBM's 90 nm CMOS logic technology. Samsung indicated that it plans to use IBM's logic technology for its system-on-chip product lines such as HD-TV, DVD, and mobile applications. The logic process may be made available in Samsung's foundry customers. There was no indication that this agreement included the eDRAM technology. The joint development is occurring in East Fishkill at IBM's 300 mm Technology Center. Each company is expected to implement the process in its own manufacturing areas. Samsung in March of 2004 was working at moving from 110nm to 100 nm technology for its DRAMs. [20]

In July of 2003, IBM discussed the deep trench capacitor DRAM structures. These have cell capacitance that remains about 40 fF even as the technology shrinks. The high cell capacitance has good retention characteristics (3.2 ms @ 105 C). The trench structure provides tolerance to variations in manufacturing and has demonstrated good immunity to various soft error mechanisms. Another advantage of the trench fabrication is that it is easily integrated into the logic process. The high temperature processes of formation are completed prior to making the high performance transistor so no performance or yield degradation of the logic devices results. The wafer can be planarized after fabrication of the trench. The BEOL process, after capacitor formation, is identical to logic only BEOL processes. The bitlines used the standard logic M1 level.[24]
The eDRAM adds only three additional mask levels to the standard logic process: two block levels and one critical level. The technology is scalable from 180 nm to 65 nm. Also the trench capacitors have excellent decoupling properties. [24]

IBM has suggested that a rule of thumb for using optimized deep trench eDRAM in an application is when 1/3 of the chip is contiguous eSRAM, it makes sense to replace it with eDRAM. The architecture of the processor also can help make the determination. If the architecture needs small fast memory then SRAM is used but if there is a 5-10% improvement in performance from doubling the L2 cache then even if it is slightly slower, it makes sense to use eDRAM. [23]

IBM 180 nm eDRAM technology:
In July of 2003, IBM had the 180 nm logic process with eDRAM qualified and in production. Target market was communications, networking and servers. [24]

The eDRAM in 180 nm technology was IBM's first external production generation of logic-based eDRAM. [24]

Its features included: [24]
-- The eDRAM was Logic Based
-- It used a deep trench storage cell
-- Row and Column repair were with laser fuses contained in the macro
-- It included BIST
-- It had a wide I/O for data bandwidth
-- Operating modes were: asynchronous EDO DRAM-like interface
    random access with demultiplexed (broadside) addressing
    page mode access (row/col addressing)

130 nm eDRAM Technology:
In July of 2003, the 130 nm logic process with eDRAM was qualified and ramping production. Target market was communications and networking, servers, printer controllers, DSP's and other standard products. [24]

Features of IBM's second generation 130 nm production eDRAM included: [24]
- Remote laser fuses with improved wireability over the macro
- BIST enhancements including SROM on-the-fly-reload and clock multiplier
- Operating modes including SDRAM like interface with concurrent access from multiple banks

In the 130 nm process the eDRAM adds four masking steps to the CMOS logic process and at 90 nm it adds three mask layers. The eDRAM technology has power advantages over SRAM and a significant decrease in SER. [23]
### Masking Steps Added for IBM eDRAM in Various CMOS Logic Processes

<table>
<thead>
<tr>
<th>Process</th>
<th>Masking Steps Added</th>
<th>Process Complexity Adder</th>
</tr>
</thead>
<tbody>
<tr>
<td>130 nm</td>
<td>4</td>
<td>20%</td>
</tr>
<tr>
<td>90 nm</td>
<td>3</td>
<td></td>
</tr>
</tbody>
</table>

IBM also estimated a 20% increase in process complexity due to the addition of the deep trench capacitor and indicated that needs to be balanced against the 1/3 to 1/4 area per megabit of the eDRAM compared to the eSRAM. Performance is close to that of SRAM and the power is significantly less than SRAM. [27]

### Features of IBM 130 nm Embedded DRAM Macro [27]

- **Technology**: 130 nm
- **Density**: 144 Mbit
- **Added Masks**: 4 (over CMOS Logic)
- **Die Size**: 121 mm²
- **Cycle Time**: 5.6 ns
- **Data Rate**: 1.4 Gbps
- **Write Technique**: Early Write
- **Area DRAM/SRAM**: 1/3

In June of 2003, Analog Devices announced that its 130 nm TigerSHARC Processor would use eDRAM developed jointly with IBM and that IBM would serve as the foundry for the IC's.

In August of 2003, Analog Devices discussed their cooperation with IBM for development of the 2nd generation TigerSharc DSP's in 130 nm CMOS 8SF technology. To reach performance levels of 4.8 billion MACs and 3.6 billion FLOPS the TS201 DSP core was redesigned to run at 600 MHz and 24 Mbits of eDRAM was added. Two other versions, the TS202 with 12 Mb of eDRAM and the TS203 with 4 Mb of eDRAM ran at 500 MHz. A 128 bit on-chip buses provided bandwidth of 38.4 Gbytes/s between macros which include: 2 floating point MACs, 2 ALUs, and an I/O processor that controls 14 DMA channels. Power consumption is about 2.5W running at 500 MHz. [43] [42] ADI indicated that its IBM collaboration is planned to continue to the 90 nm and 65 nm eDRAM nodes. [44]
90 nm eDRAM technology:
An experimental 800 MHz eDRAM in 90 nm technology was also shown in February of 2004. This device tried to simplify the eDRAM process and thereby reduce the process cost adder. It used a transfer gate made from the 2.2nm thick gate oxide 1.5V I/O device that is already part of the 90 nm logic process. This avoids a third oxide thickness for the DRAM access device. The macro has a concurrent refresh mode, an in-macro refresh scheduler, a redundancy allocation logic and a 4 time command multiplier. The 2.2 nm logic array transistor supplier about 25% more current that the normal 5.2 nm device so that 80 mA of sensing signal can be obtained for a 3.2 nm random access cycle time without using destructive read architecture. Since the thin oxide pass device results in a short data retention time of 64 us, a concurrent refresh mode is used where the macro enables simultaneous memory access and refresh.[22]

IBM's 90 nm Cu-08 ASIC process with compilable embedded DRAM offers tools, logic library and an embedded DRAM compiler. The compiler supports multibanking operation. There is an embedded Fuse capability for SRAM redundancy. Density optimized embedded DRAM is offered in 584 Kb to 73 Mb in 584 Kb increments. Multiple macros are possible per chip. The cell size 0.185 μm² and a 83Mbit macro is 27.17 mm². Random access time is 6 ns with 7 ns cycle time. Maximum data rate is 500 MHz. Data bus width is 146 bits to 1168 bits. The fast eDRAM macro is offered in 584 Kb to 36.5 Mb in 584 Kb increments with multiple macros per chip. A 36.5 Mb macro size is 18.23 mm². Random access time is 4.3 ns, random cycle time is 4.5 ns and maximum data rate is 444 MHz. Data bus is 146 bits to 1168 bits. [28]

IBM's 90 nm copper interconnect, Cu-08, ASIC technology has drawn gate length of 70 nm, low-k dielectric, up to 73-Mbit per macro of trench capacitor embedded DRAM, library options and eight levels of copper. IBM's 130 nm copper process has 4-8 levels of copper interconnect and their 180 nm copper process has 2-6 levels of copper interconnect.[29][39]

The IBM Cu-08 90 nm ASIC technology product specifications include[30]:
- L drawn = 70 nm
- Up to 72-million wireable gates
- Low-k dielectric
- Trench capacitor embedded DRAM, with up to 73 Mb per macro
- compilable high performance SRAM macros
- Multiple logic library options for performance and power optimization
- Power supply: 1.0 V with 1.2-V option
- I/O power supply: 3.3 V (triple oxide option); 2.5 V (triple oxide option); 1.8 V; 1.5 V
- Power dissipation: 0.006 μW/MHz/gate
- Gate delays: 21 picoseconds (2-input NAND gate)
- Eight levels of copper for global routing
- Automatic gate array fill of free space for quick-turn engineering-change options
70nm eDRAM technology:
Also in June of 2003, IBM discussed scaling vertical transistor DRAM cells to 70 nm using a functional 512Mb DRAM prototype at 110 nm half-pitch ground rules. The two key enabling technologies are high aspect ratio STI fill and low resistance metal deep trench fill along with some minor cell modifications consisting of reducing the parasitic capacitance, cell-to-cell interactions and cost. Introduction of a bordered contact reduced the bitline capacitance by 48% and together with a tungsten stud simplifies the process and reduces the cost penalty of the vertical transistor to less than 3% for a four level metal process. A reduced bitline capacitance recovers some cost as does the use of fewer sense amplifiers. [25]

The nine step process flow is shown below. [25]

Array / support integration Process Flow [25]
• Deep Trench Capacitor and pass gate
• Isolation Trench Fill and Planarization
• Array Top Oxide (ATO) planarization
• Array Poly deposition
• Masked strip of array poly and ATO in support device areas
• Support device gate oxide and poly dep.
• Masked etch of logic gate poly in array
• PC patterning and bordered contact
• Dual Damascene W bitline for array

Trench eDRAM on SOI:
In December of 2003, IBM discussed a trench eDRAM embedded in unpatterned SOI built in IBM's high performance 130 nm SOI logic technology. A low leakage floating body array pass transistor was used. Wafer repairable yield was as high as 67% for 524 Kbit Array Diagnostic Monitors (ADM). 16 Mbit macros were built and were fully repairable. Retention time was on the order of 80 ms. The goal was a simple and low cost integration of trench capacitor eDRAM with high performance SOI logic for use in SoC chips. This technology is intended for production use at 90 nm and smaller geometries.[26]

The main problem in building eDRAM in SOI is the poor data retention characteristics due to floating body effects of a pass transistor built on the SOI substrate. This problem had been previously avoided by the process of building the eDRAM in islands of bulk CMOS patterned using SIMOX in SOI logic. This process was both complex and had an area penalty. In this technology the floating body problems are controlled by using grounded bitline precharge and by restricting specific circuit operations of the eDRAM.[26]
The trench capacitor is made in the SOI wafer by etching the trench directly through the BOX layer. The capacitor plate is connected by N-band contacts in a diffusion guard ring surrounding the array. The collar oxide is eliminated. The low leakage NMOS pass transistors are decoupled from the SOI NMOS transistors and formed using its own separate well process. The savings over the bulk island approach was estimated at 25%-30%. The metal wiring used the standard 130 nm BEOL technology. The leakages due to buried strap junction, bitline contact, plate to p-well, trench sidewall and cell-to-cell are eliminated. The elimination of these leakage paths was thought to compensate for the increased leakage of the floating body array transistor. Unlike a bulk eDRAM array transistor, an SOI array transistor cannot be back-biased to decrease off-state leakage. A comparison of leakage paths between bulk and SOI eDRAM cell are shown below.[26]

Microsoft's Xbox2 console will use three IBM PowerPC G5 class 64-bit processors which will be made in 65 nm technology at IBM. It was not reported if these processors would use eDRAM. [46]

Sony indicated in February of 2004 that they plan to establish mass production of chips using 65 nm process technology on 300 mm wafers both by having their own fab and by collaborating with Toshiba for eDRAM technology and with IBM for SOI technology. They expect to invest $340 billion in a 300 nm SOI line at IBM's Fishkill wafer fab. The cell processor is expected to be made eventually in 65 nm technology.[47]

In October of 2004, it was reported that IBM was suffering yield problems in their 300mm fab in East Fishkill, N.Y. which was running 130 nm and 90 nm processes at the time. They were boosting wafer output to improve deliveries. [49]

In February of 2005 at the ISSCC, IBM, Sony and Toshiba showed their Cell processor design. Coding is now being done for the Sony Playstation 3 which will use the Cell. IBM plans to use the CPU in the Xbox Next and a workstation. It is of potential interest to Apple computer. The Cell MPU is a 64-bit Power-based multi-core system which is also multi-threaded. Each core can run a single operating system independently of the others. It will ship initially in a 90 nm SOI technology.[48]
4.8 Infineon

Infineon is a mainstream commodity DRAM supplier with P-SRAM and some eDRAM. They make both the Mobile DRAM and the Cellular RAM which is a P-SRAM, that is a DRAM with an SRAM interface and access modes. They use a deep trench DRAM technology they jointly developed with IBM over several generations.

Infineon makes Cellular RAM from 32-Mb to 128-Mb. It has a 1.8C core and I/O and an asynchronous SRAM interface with page and burst mode operation. On-chip logic includes a temperature sensor to improve internal refresh control. The part does not need external refresh during operation. [144]

In October of 2004, Inotera, a joint venture of Nanya and Infineon announced volume production capacity of 24,000 wafers per month in their joint 300 mm DRAM wafer fab in Taiwan. The fab is running Infineon's 110 nm trench technology. Products running include a 256-Mb DDR SDRAM and a 512-Mbit DDR2 SDRAM. The second stage for the 300 mm facility was expected by end 2005 and is expected to bring another 25,000 wafers/month on line.[55]

In April of 2004, Infineon announced a capacity expansion at its Virginia subsidiary starting with production of advanced DRAM chips on 300 mm wafers in early 2005 in 110 nm technology with an early transition to 90 nm. This expansion in Richmond was intended to allow Infineon to accelerate a shift from memory to logic products at their 200 mm plant in Dresden. The 200 mm plant in Richmond will continue to operate at full capacity. After the initial expansion the site will be able to process 25,000 wafer starts per month in 300 mm technology with operations starting in early 2005. A further expansion is possible. [56]

In December of 2004, Infineon was running most of its DRAM production on 110 nm process using a trench capacitor cell.[57]
4.9 Kawasaki Steel

Kawasaki Steel has some embedded DRAM capability. Kawasaki makes ASICs, USB controllers, CAMs and other chips for connectivity and communications applications. Kawasaki’s ASIC business is targeted at the network, telecommunications, and mobile computing areas.[58]

In 2004 Kawasaki Steel licensed the MoSys 1T-SRAM eDRAM technology for use as embedded memory in their ASIC’s and SoC. for products such as digital cameras, set-top boxes and digital TV’s.[104]

In March of 1999, Kawasaki Steel agreed with UMC to provide foundry services for Kawasaki’s ASIC and standard products line at 180 nm including copper and low-k dielectric. Kawasaki started ASIC processing with 250 nm technology in 1999 and planned a second fab for 180 nm which was subsequently cancelled after forming the agreement with UMC that future production that exceeds Kawasaki’s current fab would be run at UMC. As part of the agreement, Kawasaki made a capital investment in Nippon Foundry, which is UMC’s newest fab. The agreement gives Kawasaki access to 250 nm, 180 nm and 250 nm eDRAM processes at UMC.[58]

4.10 LSI Technology

LSI has 130 nm and 180 nm CMOS logic technology with plants located in the US and in Japan. They make IC’s for DVR, HDTV, set-top boxes and video editing. In May of 2003, MoSys announced that LSI Logic was making IC’s for DVD applications using the MoSys 1T-SRAM eDRAM technology.[59]
4.11 Matsushita

In February of 2005, Matsushita discussed a striped trench capacitor (STC) technology for a logic based eDRAM macro made in 150 nm technology. A schematic cross-section of the STC cell is shown below. [61]

![Capacitor Oxide](image)

This cell is a simplified trench cell similar in concept to the 1T-SRAM-Q cell. Features of this cell are shown in the table below.[61]

<table>
<thead>
<tr>
<th>Features of 150 nm Shallow Trench Capacitor eDRAM Macro [263]</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technology</strong></td>
</tr>
<tr>
<td><strong>DRAM Cell</strong></td>
</tr>
<tr>
<td><strong>Macro Size</strong></td>
</tr>
<tr>
<td><strong>Organization</strong></td>
</tr>
<tr>
<td><strong>Random Cycle Time</strong></td>
</tr>
<tr>
<td><strong>Refresh Period</strong></td>
</tr>
</tbody>
</table>

The eDRAM macro was dual ported and interleaved. One additional mask was required added to the CMOS logic process to make the striped trench capacitor. The capacitance was 10 fF by utilizing both side edges in each silicon trench. [61]

Matsushita makes chips for its consumer system applications which include: TV, DVD, PC and most other consumer electronics systems.

In February of 2005, Renesas and Matsushita discussed target applications of the next generation of the logic-based MIM eDRAM in 90 nm technology as being multimedia driven digital consumer electronics specifically multimedia mobile applications such as high end cell phones, PDA's, etc. [60]
4.12 Micron

Micron is a mainstream DRAM manufacturer. Their DRAMs are used in computers, communications, aerospace, automotive, office automation and video games.

Micron makes the Cellular RAM which is a DRAM with an SRAM interface for the mobile handheld system markets. In July of 2004, Micron Technology started producing 128-Mbit PSRAMs of the CellularRAM type. They indicated that in mid 2004 PSRAMs have overtaken 6T SRAMs in cell phones with a peak of 60% of the RAM market for cell phones.[62]

In 2003, Micron described a 110 nm eDRAM technology which used a stacked Al2O3 MIM capacitor with 0.1um2 cell size. High performance logic circuits were obtained by separation of the gate pattern at the memory cell and peripheral logic region. The MIM capacitors used a Al2O3 dielectric process which controlled the process temperature. Cell performance was improved by using W wordline, CoSi2 plug and W bit-line. The logic process has 7 levels of copper and low-k ILD. [140]

4.13 NEC

NEC is a former DRAM manufacturer who supplies ASIC's with eDRAM.

NEC 90 nm eDRAM Technology:
In March of 2005, NEC Electronics announced they had started production with a metal insulator metal "MIM2" capacitor 90 nm eDRAM technology. The second generation 90 nm MIM capacitor uses a high-k ZrO2 dielectric material. It is configured in a capacitor-over-bitline (COB) structure as shown in the figure below. NEC indicated that the ZrO2 capacitor would also be used for the 65 nm and 45 nm eDRAM processes. Target applications include: high end cell phones and gaming devices. A full line-up of macro's for the 90 nm ASIC CB-90 process are expected to be ready by September of 2005. [66][70]

In March of 2005, NEC and MoSys announced that they had agreed to extend the use of 1T-SRAM in pending ASIC consumer applications made in NEC’s 90 nm technology. [75]

In November of 2003, MoSys announced that they had ported their 1T-SRAM-Q (quad density) technology to NEC's 90 nm logic process and that initial silicon verification had been achieved for the 1T-SRAM-R (recessed capacitor).[65]
The relationship between MoSys and NEC has spanned multiple process generations since 1999. The 1T-SRAM-Q technology has a bit cell size of 0.3 um2 in 90 nm logic. One additional non-critical mask is added in the "Q" technology to the conventional logic process. The "Q" technology also has error correction (ECC) which can improve yield thereby potentially eliminating laser repair and soft errors.[65]

The characteristics of NEC's 90 nm MIM DRAM Cell are shown in the following table.

**NEC 90 nm MIM DRAM Cell UX6D [79]**
- COB
- MIM2 capacitor
- Dielectric: ZrO2
- Cell size: 0.22um2
- Cs = 16fF
- Salicided high-Ion cell Tr.
- Stacked contact
- CMOS compatible

NEC 130 nm Technology:
At Design Con 2006, NEC plans to display a 130 nm ASIC with SPI-4.2 core and 200 MHz eDRAM technology. NEC's 130 nm eDRAM macros allow embedded blocks of DRAM in ASICs. The eDRAM is fully compatible with NEC's conventional CMOS 130 nm process. It uses a cylindrical type stacked MIM capacitor structure. [68]

In NEC's eDRAM 130nm CB-130/UX5D and 150nm CB-12/UX4D cell-based technology, they offer up to 10-Mb of density in 130 nm and up to 8-Mb in 150 nm. [72]

The cell used in NEC's 130 nm eDRAM process was a stacked MIS or MIM cell. Salicide was used in the eDRAM cell as well as in the peripheral logic.[76]

**NEC UX5D DRAM Cell (130nm)[79]**
- COB
- MIM Capacitor
- Dielectric: Ta2O5
- Cell size: 0.35um2
- Cs = 16fF
- Salicided high-Ion cell Tr.
- Stacked contact
- CMOS compatible
NEC 150 nm Technology:
NEC's 150 nm eDRAM technology is based on a standard CMOS logic process. It has a Metal-Insulator-Metal Structure for the capacitor which has a capacitor-under-bitline configuration. The MIM capacitor is fabricated at a lower temperature than the widely used stacked SIS capacitor. Salicide is used in the logic devices and the DRAM cell transistors to improve performance. [23]

Characteristics of the NEC UX4D 150 nm DRAM cell are shown below along with a schematic cross-section of the cell. [79]

**NEC UX4D Cell (150nm)[79]**

- CUB
- MIM capacitor
- Dielectric: Ta2O5
- Cell size: 0.45um2
- Cs = 13 fF
- Salicided high-Ion cell Tr.
- Stacked contact
- CMOS compatible

NEC 180 nm Technology:
The NEC 180 nm eDRAM process is compatible with their conventional CMOS logic process. It uses a stacked MIS (Metal-Insulator-Silicon) capacitor structure in a Capacitor-Under-Bitline configuration. NEC has made gaming chips in this technology.

NEC Key eDRAM Technologies:
The key technologies of NEC's eDRAM cells in technologies ranging from 65nm to 350 nm is shown in the following figure. [79]

**Key Technology of NEC eDRAM Cells**

<table>
<thead>
<tr>
<th></th>
<th>UD1H</th>
<th>UD2</th>
<th>NED3</th>
<th>UX4D</th>
<th>UX5D</th>
<th>UX6D</th>
<th>UX7D</th>
</tr>
</thead>
<tbody>
<tr>
<td>350 nm</td>
<td>COB</td>
<td>COB</td>
<td>CUB</td>
<td>CUB</td>
<td>COB</td>
<td>COB</td>
<td>COB</td>
</tr>
<tr>
<td>250 nm</td>
<td>COB</td>
<td>COB</td>
<td>CUB</td>
<td>CUB</td>
<td>COB</td>
<td>COB</td>
<td>COB</td>
</tr>
<tr>
<td>180 nm</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
</tr>
<tr>
<td>150 nm</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
</tr>
<tr>
<td>130 nm</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
</tr>
<tr>
<td>90 nm</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
</tr>
<tr>
<td>65 nm</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
<td>CUB</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit line materials</th>
<th>WSi</th>
<th>WSi</th>
<th>W/TiN</th>
<th>W/TiN</th>
<th>W/TiN</th>
<th>W/TiN</th>
<th>W/TiN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Word line materials</td>
<td>WSi/Poly</td>
<td>CoSi</td>
<td>CoSi</td>
<td>CoSi</td>
<td>CoSi</td>
<td>CoSi</td>
<td>NiSi</td>
</tr>
<tr>
<td>Cell Tr. salicide</td>
<td>none</td>
<td>CoSi</td>
<td>CoSi</td>
<td>CoSi</td>
<td>CoSi</td>
<td>CoSi</td>
<td>NiSi</td>
</tr>
<tr>
<td>Capacitor type</td>
<td>PIP</td>
<td>PIP</td>
<td>MIS</td>
<td>MIM</td>
<td>MIM</td>
<td>MIM</td>
<td>MIM-2</td>
</tr>
<tr>
<td>Dielectric materials</td>
<td>Si3N4</td>
<td>Si3N4</td>
<td>Ta205</td>
<td>Ta205</td>
<td>Ta205</td>
<td>ZrO2</td>
<td>ZrO2</td>
</tr>
<tr>
<td>Max temperature</td>
<td>900°C</td>
<td>850°C</td>
<td>800°C</td>
<td>450°C</td>
<td>450°C</td>
<td>450°C</td>
<td>450°C</td>
</tr>
<tr>
<td>Ref. Dielectric of CMOS</td>
<td>SiO2</td>
<td>SiO2</td>
<td>SiON</td>
<td>SiON</td>
<td>SiON</td>
<td>SiON</td>
<td>HfO2</td>
</tr>
</tbody>
</table>
In August of 2002, NEC announced availability of their 130 nm eDRAM process based on their low-
k dielectric copper CMOS process. The eDRAM operates at 1.2V, speed is 314 MHz with 1 cycle latency and page mode of 595 MHz. It is available in an 8Mb or 9Mb hard macro as well as configurable macros. Designs in this technology are expected from communications, consumer, high end cell phones, ATM switches and routers and PC graphics cards. The upper metal layers of the ASIC can be routed over the top of the eDRAM blocks to improve timing and reduce silicon.[69]

NEC indicated that at about 90 nm the low power of the eDRAM option was attractive for applications such as mobile phones.[71]

NEC indicated in February of 2003 that they had shipped more than 6 million chips containing embedded DRAM at that time. Their eDRAM technology is claimed to be fully integrated into their ASIC technology. They claim to have shipped millions of ASICs with eDRAM. [73]

### 4.14 Philips

Philips Semiconductor designs and supplies logic chips. They have developed their own process technology as well as owning a share of TSMC and using the TSMC processes. They have in the past developed embedded DRAM technology and are currently developing advanced CMOS technology including eDRAM technology in a cooperation with ST Microelectronics, TSMC and Motorola at their joint facility in Crolles, France.

The Philips processes and the facilities running them are shown in the following table.

<table>
<thead>
<tr>
<th>Process</th>
<th>Philips CMOS Processes by Wafer Fab [81]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VSC8</td>
</tr>
<tr>
<td>Gate Length(drawn)(um)</td>
<td>.35</td>
</tr>
<tr>
<td>Gate Length(effective)(um)</td>
<td>.3</td>
</tr>
<tr>
<td>Metal Layers</td>
<td>2,3</td>
</tr>
<tr>
<td>Supply Voltage(V)</td>
<td>3.3</td>
</tr>
<tr>
<td>Interconnects</td>
<td>Copper</td>
</tr>
<tr>
<td>Gate Oxide</td>
<td>Dual(BiCMOS)</td>
</tr>
<tr>
<td>Memory Types</td>
<td>eDRAM</td>
</tr>
<tr>
<td>Production Start</td>
<td>1Q01</td>
</tr>
<tr>
<td>Fab</td>
<td>STMS Micrus</td>
</tr>
</tbody>
</table>

The STMS fab in Germany and the Micrus fab in New York were former IBM DRAM factories.
Philips makes field memories for television applications. Field memories are serial DRAM memories used in television type applications. Field memories are used in 50 Hz television such as the PAL TV standard for 100 Hz conversion. PAL is used in Europe, South America, Australia and China. Field memories are also used in NTSC TV and DVD's for progressive scan techniques. The U.S., Canada, Taiwan, Korea, Mexico and Japan has NTSC. [87][88]

Philips makes the SAA4979H/V105/6/7 which is a television sample rate converter chip with noise reduction. The chip has 3.5-Mbit of field memory, a 15 MHz 80C51 MCU with 256-kbit ROM and 4-kbit SRAM. Sample frequency is 32 MHz and 27 MHz. It was made originally in a CMOS5L (450 nm) process and scaled to 350 nm. It is a multi-rate scan rate conversion chip (50:100 Hz or 60:120 Hz) with noise reduction circuitry. It supports both digital and analog applications. It has two digital input channels for off-chip field or frame PIP processing. It also has an expansion port for use with motion estimation and compensation IC's. In this application sample frequency is 32 MHz [87][88]

Scan conversion is required because 100 Hz TV tends to place moving objects at an incorrect position. This is emphasized when pictures are filmed at movie rate which is 24 frames per second and undergo a four fold duplication to come up to 100 Hz rate. This causes the object actually seen to appear to jump, an artifact called judder. Motion estimation solves the judder problem but requires a large number of calculations. The Philips up-conversion and motion compensation IC's in Philips have gone through 3 generations of chips with embedded DRAM between 1996 and 2003. These are the SAA4991, SAA4992 and SAA4998.

The SAA4991 was a first generation motion upconversion and compensation chip in 800 nm technology with embedded DRAM called the "Melconic". It included functions for motion estimation and compensation, line flicker reduction, vertical zoom and noise reduction. It included four VSP's for motion estimation, upconversion, temporal vector, and a top level processor. It received the European Video Innovation Award in 95-96. 15 dual port 8bitx896word 33 MHz FIFO DRAM memories were used for the 15 line delay memory instances due to area and power. A dedicated line memory doubled data throughput at 33 MHz using simultaneous read and write access to the same memory address in one memory cycle. Page mode reduced power by a factor of three. A single DRAM line memory stores 896 8-b pixels, measures 1.1 mm2 and dissipates 0.5 mW/MHz at 5V. Two single port 10 bit x 4096 16,5 MHz DRAM instances were used for the field delay memory [82][84]

The SAA4992 was a second generation motion compensation chip called the "Falconic". This IC was made in a tighter 350 nm technology and had a smaller chip size in spite of 4 times the number of transistors and quadrupling the vector resolution. It has about 3-Mb of eDRAM. The increased number of transistors is primarily a result of additional on-chip memory. Algorithms used are: de-interlacing, motion compensated up-conversion, motion compensated noise reduction. [92]
In July 2003, the SAA4998 high end motion compensation/estimation chip for 100 Hz and progressive scan LCD or Plasma TV was introduced. This chip, which uses embedded DRAM, addresses format conversion and enhancement for the various frequency rates and display formats of modern television. It reduces blur and judder during fast motion sequences in film, TV and DVD. Edge dependent de-interlacing results in sharper characters and diagonal lines and motion compensated picture interpolation reduces blur. Blur is a pitfall in LCD panels. For DVD the motion compensation reduces judder. The chip does 100 Hz conversion and permits 60 Hz LCD panel use in 50 Hz regions (Europe, Asia) with judder free 50 Hz to 60 Hz conversion. It does conversion from the 24/25/30 Hz used in film and the 50/60 Hz used in video input material. It handles both interlaced and progressive scan output formats ranging from 50 to 120 Hz. It can output to DLP screens. New algorithms include: a 3-D recursive search motion estimator and a new delacing algorithm. The motion estimation and conversion algorithms from the earlier chips are used. [83][94]

Features of the SAA4998 are shown in the following table.

<table>
<thead>
<tr>
<th>SAA4998 Motion Compensation for Flat Panel LCD and Plasma TV [94]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
</tr>
<tr>
<td>Wafer Fab</td>
</tr>
<tr>
<td>Transistors</td>
</tr>
<tr>
<td>Chip Size</td>
</tr>
<tr>
<td>eDRAM</td>
</tr>
<tr>
<td>Package</td>
</tr>
<tr>
<td>Vector Accuracy</td>
</tr>
<tr>
<td>pull down</td>
</tr>
</tbody>
</table>

A cost optimized SAA4999A was also introduced which uses embedded DRAM.[83]

On 100 Hz LCD screens the SAA4998 reduces blur and permits 60 Hz LCD panels to be used in 50 Hz regions. Video is enhanced on 100 Hz Plasma displays where the motion compensation reduces judder. For movies the film is recorded at 24/25/30 Hz. The sub-pixel accuracy of the motion estimator models camera caused motion well. Motion conversion is adapted to all video and film input picture rates. It automatically recognizes the original picture rate on input video. For DVD it reduces blur and judder during fast motion sequences in film, TV and DVD. The SAA4998 family was sampling in July 2003 and was expected to begin in volume production in August of 2003.[83]

Loewe Opta, a high end TV manufacturer, indicated that they used the SAA4998 chips in their TV's which are based on matrix displays using: PDP(plasma display panels), LCD (liquid crystal displays), and DLP(Digital Light Processing - TI's digital micro-mirror-devices). They were the first company to apply this technology for the consumer market in their Spheros-42-HD launched in July of 2003.[83]
In May of 2003, Loewe announced their Spheros 42 HD 42" plasma screen TV with 1024 x 1024 pixel resolution which uses the Philips SAA4999A motion compensation technology. Various multimedia features can be added such as encrypted satellite, digital pay TV, etc. can be added and used with an activated smart card. The set is also web enabled and can add home automation control features.[83]

### 4.15 Renesas:

Renesas is the world's third largest semiconductor supplier with major market shares in microcontrollers, smartcards, and flash memory. They were formed in April of 2003 as the merger of the logic chip businesses of Hitachi and Mitsubishi. [86]

Renesas inherited the processor group of Mitsubishi which had in previous times done significant work in embedded DRAM in processing chips. They also inherited the processor group of Hitachi which has also done work in embedded DRAM. With these two microcontroller operations, Renesas became a leader in microcontrollers. Renesas indicates on their web page that they have embedded DRAM available in their ASIC IP library. [85]

Renesas is developing a capacitor under bit-line (CUB) MIM stacked cell in their advanced technologies which reduces the aspect ratio of the interconnects making the process more logic compatible. The capacitance of the MIM cell in 90 nm technology at 5 fF is lower than that of the capacitor over bit-line (COB) MIS cell at 15 fF. [90][91]

They reported on this 130 nm MIM eDRAM cell in logic-based technology in February of 2004 at the ISSCC. Technology features were:[89]

```
<table>
<thead>
<tr>
<th>Technology Features of 130 nm Logic Based MIM eDRAM[89]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology Node</td>
</tr>
<tr>
<td>Dual Tox</td>
</tr>
<tr>
<td>Ion (@ Vd=Vg=1.2V)</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>16-Mbit Macro</td>
</tr>
<tr>
<td>Cell Size</td>
</tr>
<tr>
<td>Cell Structure</td>
</tr>
<tr>
<td>Capacitor Dielectric</td>
</tr>
<tr>
<td>Macro I/O</td>
</tr>
<tr>
<td>Supply Voltage</td>
</tr>
<tr>
<td>Peak Power</td>
</tr>
<tr>
<td>Standby Power</td>
</tr>
</tbody>
</table>
```

== = © 2005 Memory Strategies International; Not for copying, redistribution, or public posting == =
In February of 2005, Renesas and Matsushita reported on the technology of a logic-based MIM capacitor eDRAM in 90 nm technology. Technology and features are shown in the table that follows.[91]

<table>
<thead>
<tr>
<th>Technology Features 90 nm Logic Based MIM Capacitor eDRAM[91]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology Node</td>
</tr>
<tr>
<td>Macro Density</td>
</tr>
<tr>
<td>Dual Tox</td>
</tr>
<tr>
<td>Access Trans Ion</td>
</tr>
<tr>
<td>Cell Capacitor</td>
</tr>
<tr>
<td>Capacitance</td>
</tr>
<tr>
<td>Cell Size</td>
</tr>
<tr>
<td>Voltage</td>
</tr>
<tr>
<td>Refresh Rate</td>
</tr>
<tr>
<td>Data Retention Power</td>
</tr>
<tr>
<td>Interface</td>
</tr>
<tr>
<td>Random Cycle Speed</td>
</tr>
<tr>
<td>Cell Leakage</td>
</tr>
</tbody>
</table>
4.16 Samsung

Samsung has shown various technical papers on eDRAM. They also make PSRAMs. In the past few years they have been attempting to expand beyond their focus on DRAMs into the ASIC with eDRAM and eFlash markets.

Their ASIC process roadmap is shown as given on the Samsung web page. Embedded DRAM is in development at the 130 nm and 90 nm technology nodes with 130 nm process release occurring at the beginning of 2004 and 90 nm process release toward the end of 2004. Their product portfolio indicates eDRAM products available at the 350, 250 and 180 nm nodes[92]

<table>
<thead>
<tr>
<th>Process</th>
<th>Technology</th>
<th>2003</th>
<th>2004</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Q3</td>
<td>Q4</td>
</tr>
<tr>
<td>Logic</td>
<td>90 nm Cu</td>
<td>1.0 V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>90 nm Cu</td>
<td>1.2 V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>60 nm Cu</td>
<td>0.85V</td>
<td></td>
</tr>
<tr>
<td>eDRAM</td>
<td>130 nm Cu</td>
<td>1.2V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>90 nm Cu</td>
<td>1.0/3.3V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.0/2.5 V</td>
<td></td>
</tr>
</tbody>
</table>

Samsung uses an optimized stacked capacitor cell for their DRAMs and their eDRAMs. In 1999, Samsung described a self-aligned pillar cell based on the 8F2 folded bit-line architecture in 150 nm technology but intended to be used in 130 nm for a 1G-bit DRAM and in 100 nm technology nodes and also suitable for integration in a logic technology. It stores 25 fF /cell with leakage current less than 1fA.cell and has good time dependent dielectric breakdown (TDDB) characteristics. [97]

In June of 2004, Samsung described their MIM capacitor DRAM intended for use in 70 nm technology. The MIM capacitor has 150 nm Toxeq and 1 fA leakage.[139]
4.17 Sanyo

Sanyo supplies application specific memories. They have focused on flash memory but have also run some applications specific chips with embedded DRAM.

In December of 2003, MoSys and Sanyo announced that Sanyo would license the MoSys 1T-SRAM for use in Sanyo's consumer product SoC designs.[98]

4.18 SMIC

SMIC has the MoSys CMOS logic compatible eDRAM for use in their logic processes.

In May of 2003, SMIC and MoSys announced that the MoSys 1T-SRAM silicon had been verified on SMIC's 180 nm logic foundry process for use in SoC designs.[100]

In July of 2004, MoSys and SMIC announced that SMIC would use the MoSys 1T-SRAM-R technology in SMIC's 130 nm process and that the silicon has been verified in this process for use by SMIC's foundry customers. This technology uses a planar DRAM cell and error correction in the macro.[99]

4.19 Sony

In May of 2005, EE Times reporting on the papers to be shown at the VLSI Technology Symposium in June of 2005 noted that Toshiba and Sony will discuss a 256-kbit eDRAM test chip in 45 nm CMOS logic technology with a 0.069 um2 cell size. Al2O3 was used for the capacitor dielectric. [141]

In January of 2005, Sony described a microprocessor made in 180 nm CMOS eDRAM technology for high performance audio and video in multipurpose handheld PDA applications with 128-bit wideband 64-Mb eDRAM. The processor used a dynamic voltage and frequency management scheme with leakage power compensation. Movie applications were targeted. Power consumption targeted for these applications is typically 250 mW including 75 mW for audio, 50 mW for scheduling and 3 mW for standby. The processor has four 128-bit data width 16-Mb eDRAM macros. Processor blocks are connected to the eDRAM by a 128-bit bus. A 2-D graphics engine is included on the chip. The maximum data transfer rate of the wideband bus is 7.86 GB/s. [142]

In February of 2001 Sony announced the 150 MHz graphics rendering processor with 256Mb (280-Mb) of embedded DRAM for their upgraded Playstation2 gaming system. The 180 nm 6 metal CMOS chip had a chip size of 21.3 x 21.7 mm2. [105]
Also in February of 2001, Sony and United Memories showed a 256Mb eDRAM macro for a 3D graphics engine assumed to be the Playstation2 processor discussed above. The chip is divided up into 16 16Mb eDRAM macros. Features of this technology are shown in the table below: [106]

### Sony Playstation Graphics Rendering Processor with 256Mb of eDRAM [106]

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>180 nm</td>
</tr>
<tr>
<td>Chip Size</td>
<td>21.3 x 21.7 mm²</td>
</tr>
<tr>
<td>eDRAM Macro</td>
<td>256Mb</td>
</tr>
<tr>
<td>Macro Increments</td>
<td>16 16Mb eDRAM macros</td>
</tr>
<tr>
<td>Cell Size</td>
<td>.37um²</td>
</tr>
<tr>
<td>Macro Size</td>
<td>15.75 mm²</td>
</tr>
</tbody>
</table>

In February of 2004, Sony discussed a Graphics Synthesizer with 32-Mbytes of eDRAM made on a 180 nm process for the Sony Playstation. The chip had 287.5 million transistors and measured 462 mm². [104]

In December of 2002, Toshiba and Sony announced a 65 nm CMOS process technology for eDRAM. The two companies were in joint development of 90 nm and 65 nm CMOS process technology initiated in May of 2001. The cell size in the 65 nm technology is 0.11um² allowing a 256-Mbit eDRAM. The process used low-K material with dielectric constant around 2.7. [102]

In April of 2003, MoSys announced that Sony would be using the MoSys 1T-SRAM technology in Sony's fab in Kyushu, Japan. Sony already used the MoSys 1T-SRAM in their consumer products. [101]

In February of 2004, Sony announced its 90 nm technology processor for the Sony Portable Playstation. Sony and United Memories discussed an eDRAM for a mobile personal consumer application requiring high speed graphics and low power. We assume it is the memory for the portable Playstation. [107]

The characteristics of this eDRAM are shown in the following table. [107]

### 16Mb eDRAM for Sony SPS [266]

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>90 nm 6M CMOS</td>
</tr>
<tr>
<td>Cell Technology</td>
<td>Trench, 40 fF capacitor</td>
</tr>
<tr>
<td>Cell Size</td>
<td>0.195 um²</td>
</tr>
<tr>
<td>Macro Density</td>
<td>16-Mb</td>
</tr>
<tr>
<td>Macro Area</td>
<td>9.1 mm²</td>
</tr>
</tbody>
</table>
In 2003, Toshiba and Sony discussed a version of the IBM "MINT" trench cell for the 65 nm technology node for integration in their CMOS5 SoC technology. The demonstrator was an 8-Mb DRAM. They used tapered BF$_2$ implantation without an additional mask step. Cell size is 0.11um$^2$. Three layers of Cu were used with 3 layers of hybrid low-k material - SiLK/BD/BLOk. The deep trench capacitor is 6 um deep with capacitance of 26 fF. The wordline is silicided for lower resistance and the storage node side is blocked for the Ni silicide operation. A tapered BF$_2$ implantation for the DRAM cell region is done after GC sidewall oxidation. The metal 1 dielectric is SiLK and the intermediate layer is 100 nm half pitch copper dual damascene interconnects with hybrid low-k material - SiLK/BD/BLOk. [108]

Four additional process steps are required for the embedded DRAM above those required for the CMOS logic process. These steps are: DT formation, DRAM cell well formation, DRAM cell tapered implant and source/drain formation and salicide block formation.[108]

### 4.20 ST Microelectronics

STM has indicated that they have an embedded DRAM technology which only adds a few masks to the conventional CMOS logic process to help reduce cost. While only a few specific examples could be found, it is clear that the efficiency of offering eDRAM to the printer market means that there were probably other examples which were not found in the literature.

STM has indicated that they have a large variety of processes optimized for specific applications that can be integrated on top of pure CMOS for various SoC chips. All of their production processes have been indicated as having an eDRAM option.

In 2002, STM indicated that at the Crolles2 facility the digital core processes that would be available included embedded DRAM which will be available in the 90 nm node and beyond. [113]

STM indicated that their advanced 130 nm process is specifically designed for maximum flexibility in embedding IP modules including: high density SRAM, eDRAM, eFlash, high speed MCU and analog. They developed a specific version of the 130 nm HCMOS9 process with eSRAM and eDRAM capability in support of hard disk drive SoC applications. This process also has specific options to support Read/Write Channel integration. The Super10 Hard Disk drive controller has some versions that use eDRAM. [112]
They also indicated that the eDRAM in 180 nm technology used only two additional mask layers over standard CMOS logic. [114]

Two of STM's product lines in their Peripheral Products group appear to use eDRAM. These are the Super10 Nova hard disk drive controller made in STM's 130 nm technology and the printer controller.

They have a specific version of the HSMOS9 process made with features for hard disk drives with eDRAM and eDRAM capability along with a high speed Super10 MCU and analog circuitry. The Nova Disk Manager chip includes a disk controller, 150 MHz Super10 DSP and eDRAM intended to increase the memory access bandwidth. The 16-bit wide e-DRAM interface is capable of 225 MB/s bursts permitting sustained data transfers between the DMA interface and the read channel with concurrent accesses for DRAM refresh, ECC, servo table management, cache table access, detect list searches and general DSP access. The "enhanced Super10" provides a set of features specially tailored for the hard Disk Drive Market. External power supply is 3.3V and internal power supply is 1.8 V. [111][112]

In March of 2001, STM announced that Quantum, the Hard Disk Drive company, (now Maxtor) had chosen STM's Super10 DSP for a new hard disk drive. This System-on-Chip in 180 nm technology would include: the Super10 DSP core, a hard disk controller, 4-Mbit of embedded DRAM and various interface functions. STM was also to supply the other chips for this drive including: read/write channel, head preamplifier, motion control combo and firmware for booting Windows OS. STM was to produce the chip in 180 nm CMOS technology with sample delivered to Quantum in 1H01. [109]

In April of 2003, STM started production of a Digital Printer Engine with embedded DRAM in 180 nm technology. They also announced a new digital printer engine SoC taped out in 130 nm technology. They had previously announced contracts with two leading printer manufacturers to develop system-on-chip solutions with embedded DRAM memory for the digital printer engines' used in inkjet printers. [110]

In June of 2004, STM showed a capacitorless DRAM in 130 nm technology that they have in development in Crolles. This 1T DRAM cell has been developed on bulk silicon substrate and is fully compatible with integration with CMOS logic. [115]

While previous capacitorless DRAM cells have been shown of partially depleted SOI, this cell is constructed on a triple well structure NMOS FET. Cell Size is 10F²/bit. One additional non-critical mask and three process steps are added to conventional CMOS.
A cross-section of this cell is shown in the following diagram.

STM Capacitorless DRAM on Bulk NMOSFET[115]

The main challenge with capacitorless DRAM cells has been that they are made on SOI substrates which are not yet common. Where SOI is the basis of the CMOS logic process, then such an eDRAM could prove to be useful.

In August of 2002, STM, Philips and Motorola announced their 90 nm CMOS design platform based in the Crolles2 project in Crolles, France. The drawn gate length was 90 nm with poly width of 65 nm and metal pitch of .28um. It has dual transistor and dual gate oxide to enable control of power and leakage with performance, uses dual damascene copper for the interconnects, and a low k dielectric. Embedded memory includes: high density SRAM, dual port SRAM, register files, and eDRAM modules. They forecast having the first 90 nm silicon on 300 mm wafers at Crolles by the end of 2002.[119][120]

The CMOS090 library platform includes: Two standard cells libraries - one optimized for power and one for performance, densities of more than 400Kgates per mm², core power supply 1.0V or 1.2V, and embedded memories including 6T-SRAM, dual port, register files and ROM compilers. [119]

A fully compatible low-cost process variant allows up to 32-Mbit of embedded DRAM with a density of 0.5mm² per Mbit. [119]

STM offers digital standard cell libraries from 250nm down to 90nm. As shown in the following chart of these libraries, the CMOS090 90nm cell library offers the embedded DRAM option. [118]
STM Digital Standard Cell Libraries [129]

<table>
<thead>
<tr>
<th>PRODUCT PROCESS</th>
<th>HCMOS7</th>
<th>HCMOS8</th>
<th>HCMOS9</th>
<th>CMOS090</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell Library</td>
<td>CB55000</td>
<td>CB65000</td>
<td>CB75000</td>
<td>CB85000</td>
</tr>
<tr>
<td>L drawn (μm)</td>
<td>0.25μ</td>
<td>0.18μ</td>
<td>0.13μ</td>
<td>90nm</td>
</tr>
<tr>
<td>Number of Metal Levels</td>
<td>6</td>
<td>6-8</td>
<td>6-9</td>
<td></td>
</tr>
<tr>
<td>Gate Density (Kgates/mm²)</td>
<td>30</td>
<td>85</td>
<td>200</td>
<td>430 (hi density)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>350 (hi speed)</td>
</tr>
<tr>
<td>Nominal Vdd (V)</td>
<td>2.5</td>
<td>1.8</td>
<td>1.2</td>
<td>1.0V/1.2V</td>
</tr>
<tr>
<td>Power Dissipation (μW/MHz/gate/SL)</td>
<td>0.1</td>
<td>0.03</td>
<td>0.024</td>
<td>-</td>
</tr>
<tr>
<td>ND2 with FO=1 (ps)</td>
<td>65</td>
<td>35&lt;</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Embedded Memory</td>
<td>SRAM</td>
<td>SRAM</td>
<td>SRAM</td>
<td>SRAM</td>
</tr>
<tr>
<td>ROM</td>
<td>ROM</td>
<td>ROM</td>
<td>ROM</td>
<td>ROM</td>
</tr>
<tr>
<td>Flash</td>
<td>Flash</td>
<td>Flash</td>
<td>Flash/RAM</td>
<td>DRAM modules</td>
</tr>
<tr>
<td>eDRAM</td>
<td>eDRAM</td>
<td>eDRAM</td>
<td>eDRAM</td>
<td>eDRAM</td>
</tr>
<tr>
<td>Year Entered Production (approximate)</td>
<td>98</td>
<td>00</td>
<td>02</td>
<td>04</td>
</tr>
</tbody>
</table>

STM also indicated that their ASIC services in 180 nm technology include eDRAM options.[121]

STM makes a line of PSRAMs which are delivered in modules with flash memory for use in mobile terminals. These include 16Mb, 32Mb and 64Mb PSRAMs. These parts are made in 130 nm, 150 nm and 180 nm technologies. The source used for the following table was updated in July of 2004. [116][117]

Characteristics of 16Mb - 32Mb Asynchronous PSRAM

<table>
<thead>
<tr>
<th>Technology*</th>
<th>180</th>
<th>180</th>
<th>150</th>
<th>180</th>
<th>130</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density(Mb)</td>
<td>16</td>
<td>16</td>
<td>32</td>
<td>32</td>
<td>4</td>
</tr>
<tr>
<td>Organization</td>
<td>1Mb x 16</td>
<td>1Mb x 16</td>
<td>2Mb x 16</td>
<td>2Mb x 16</td>
<td>256Kx16</td>
</tr>
<tr>
<td>Operating Volt(V)</td>
<td>1.8(1.7-1.95)</td>
<td>3.0(2.7-3.3)</td>
<td>1.8(1.65-1.95)</td>
<td>3.0(2.7-3.3)</td>
<td>1.8(1.65-1.95)</td>
</tr>
<tr>
<td>Read Cycle(ns)</td>
<td>70</td>
<td>60</td>
<td>70</td>
<td>70</td>
<td>70</td>
</tr>
<tr>
<td>Op Temperature(C)</td>
<td>-30+85</td>
<td>-30+85</td>
<td>-30+85</td>
<td>-30+85</td>
<td>-40+85</td>
</tr>
<tr>
<td>ICCmax(mA)</td>
<td>15</td>
<td>20</td>
<td>25</td>
<td>30</td>
<td>6</td>
</tr>
<tr>
<td>ISTBmax(μA)</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>8</td>
</tr>
</tbody>
</table>

*Estimated from the parameters given.
Comparing the characteristics of the PSRAMs and the SRAM, note that the operating temperature range of the PSRAMs is lower than the 6T SRAM. Also note that the operating current of 8 of the 1.8V 4M SRAMs would have been 48mA whereas the single 1.8V 32Mb PSRAM has an operating current of 25 mA which is about half the operating current. The PSRAMs power down automatically when deselected. The refresh is hidden so that operation is similar to that of the SRAM. They have temperature controlled self refresh and partial array self refresh which reduces the power dissipation of the PSRAM still further.

4.21 Toshiba

Toshiba has been a supplier of ASIC and custom logic chips with eDRAM for many years. The following subsections consider recent Toshiba eDRAM technology by generation.

45 nm eDRAM Technology
In June of 2004, Toshiba described their 45 nm CMOS technology with a 0.069 um2 trench capacitor eDRAM and a 0.247 um2 six transistor eSRAM. The eDRAM had a surface strap and used a high-k dielectric for the capacitor dielectric. [138]

In June of 2003, Toshiba described an embedded capacitorless DRAM cell on SOI wafers with mass production on SoC expected to begin in 2006 for the 45 nm technology node. The logic on SOI is fast and low power and the capacitorless DRAM cell is smaller than the DRAM with a capacitor. The target application is broadband network applications. [122]

65 nm eDRAM Technology:
In December of 2003, Toshiba and Sony discussed a version of the MINT cell for the 65 nm technology node for integration in their CMOS SoC technology. The demonstrator was an 8-Mb DRAM. They used tapered BF2 implantation without an additional mask step. Cell size is 0.11um2. Three layers of Cu were used with 3 layers of hybrid low-k material - SiLK/ BD/BLOk The deep trench capacitor is 6 um deep with capacitance of 26 fF. The wordline is silicided for lower resistance and the storage node side is blocked for the Ni silicide operation. A tapered BF2 implantation for the DRAM cell region is done after GC sidewall oxidation. The metal 1 dielectric is SiLK and the intermediate layer is 100 nm half pitch copper dual damascene interconnects with hybrid low-k material - SiLK/BD/BLOk. A cross-sectional TEM of the deep trench and the copper structures is show in the figure below. [137]

Four additional process steps are required for the embedded DRAM above those required for the CMOS logic process. These steps are: DT formation, DRAM cell well formation, DRAM cell tapered implant and source/drain formation and salicide block formation.[137]
In December of 2002, Toshiba and Sony announced a 65 nm CMOS process technology for eDRAM. The two companies were in joint development of 90 nm and 65 nm CMOS process technology initiated in May of 2001. The cell size in the 65 nm technology is 0.11 um2 allowing 256-Mbit eDRAM. The process used low-K material with dielectric constant around 2.7. [129]

Toshiba is also working on advanced process development with IBM and Sony and with other alliances but these are separate from the TC300 development. Toshiba collaborated with Fujitsu on SoC at the 90 nm and 65 nm node. [124]

90 nm eDRAM Technology:
In January of 2003, Toshiba announced the launch of their 90 nm TC300 family based on Toshiba's CMOS4 modular process. The process has 65 nm drawn gates, 11 layers of copper interconnect and low-k dielectric. An aluminum version was introduced first with copper following. The modular process permits mixing of mixed signal, eDRAM and various specialty IP on a chip. The process has two types of eDRAM one optimized for speed and the other for density. The TC300 also supports full chip hierarchical design supporting leading edge tools such as the Cadence and Magma design environments. Target Applications include high speed networking and server applications, digital multimedia and low power portable wireless. [122][127]

The Toshiba TC300 process will be equipped from the start to produce eDRAM. Toshiba indicated that the typical design was mixed signal and there were only 6 mask steps out of 30-40 different between mixed signal and eDRAM. Toshiba indicated that first samples of 90 nm SoCs have shipped to a consumer electronics customer and used the eDRAM option. The 90 nm eDRAM CMOS4 process being built in Toshiba's Oita, Japan facility. [124]

The 90 nm CMOS4 technology doubles gate density over the CMOS3 to 400,000 gates per sq. mm., gate delay is 11 ps and power consumption is half at 7 nW/MHz/gate. The eDRAM will be in blocks of up to 32 Mbit for the 33 ns access time version and up to 16-Mb for the 8-10 ns versions. Fast access cores will target high speed narrow width applications such as network switches with SDRAM with 256 bit bus will target streaming media applications. [124][127]
In February of 2005, Toshiba discussed a 90 nm SOI "capacitorless" DRAM using an experimental 2Mb macro. Access time was 18.5 nm, cell size was 6F2 where F = 165 nm, cell size was 0.17 um2, with 90 nm 6M SOI CMOS technology. A 128-Mb test chip is being built. [130]

130 nm ASIC eDRAM Technology:
In February 2003, Toshiba introduced an MPEG4 encoder and decoder chip for multimedia 3D graphics in cell phones made in 130 nm CMOS technology. The TC35285XBG part had a 20-Mb eDRAM macro. The chip supports graphics rendering, shading, texture mapping, and special effects. It included a JPEG codec for a 2-megapixel camera and an LCD control circuit. Samples were expected in 2Q04 with volume production in 3Q04.[131]
110 nm P-SRAM: Toshiba offers P-SRAM from 32-Mb to 128-Mb densities and is widely used in cell phone applications. Toshiba's P-SRAM has DRAM array and an asynchronous SRAM external interface. It is based on the COSMORAM specification defined by Toshiba, NEC, and Fujitsu. Toshiba intends to support up to 256Mb density in 110 nm DRAM technology during 2005. [125]

In November of 2002, Toshiba announced their TMPR9961 processor with 800 MHz MIPS64 core and 32-Mbytes of logic process eDRAM. The part is targeted at graphics oriented embedded applications such as automotive navigation systems, set-top-boxes, and digital televisions. The eDRAM is used as video memory while the caches for the MIPS core use SRAM.[128]

In January of 2003, Toshiba announced a 128-Mb PSRAM made in 175 nm technology. The chips have a standby current of 250 uA, 70 ns access time, and 3 uA deep power-down. Partial refresh mode lowers power during standby. The parts have higher density than SRAMs, high speed and low power consumption making them suitable for mobile phones. The parts sampled in January of 2003 with production following in March of 2003 at a monthly volume of 200,000 pieces. [126]

Toshiba ASIC with eDRAM: TC300: (Networking, Server, Multimedia, Portable Wireless)
In 2003, Toshiba introduced their 90 nm copper, low-k TC300 family with mixed signal, eDRAM and various specialty IP modules mixed on a chip. The process has two types of eDRAM one optimized for speed and the other for density. Target applications for the high speed options for Toshiba's 90 nm TC300 ASIC family included high speed networking and server applications, digital multimedia. Target applications for the low power option included low power portable wireless. [122][127]

MPEG4 En/Decoder for Multimedia Cell Phones:
In February 2003, Toshiba introduced an MPEG4 encoder and decoder chip for multimedia 3D graphics in cell phones made in 130 nm CMOS technology. The TC35285XBG part had a 20-Mb eDRAM macro. Chip size was 6.56mm x 6.56 mm. The chip supported graphics rendering, shading, texture mapping, and special effects. It included a JPEG codec for a 2-megapixel camera and an LCD control circuit. Samples were expected in 2Q04 with volume production in 3Q04.[131]

By June of 2003, Toshiba was beginning to struggle with integrating the eDRAM structure into the advanced technology nodes. They presented a trench eDRAM with a FINFET transistor. The test chip was in 130 nm technology. [136]
4.22 TSMC

TSMC is a pure play foundry that focuses on providing silicon for fabless semiconductor companies as well as for larger IDM's. They have a range of low cost eDRAM options discussed below.

130 nm Logic Technology with Embedded DRAM:
The 130 nm logic technology supports the 1T SRAM (1T-P DRAM) technology. Their 130 nm process offers up to 8 metal layers with either low-k or FSG processes. By the end of 2003, 130 nm production accounted for 20% of revenue with volume production on both 8-inch and 12 inch wafers. At that time 500k 130 nm wafers had been shipped. Both 2.5V and 3.3V I/O's are available.[133]

90 nm Logic Technology with Embedded DRAM:
TSMC's 90 nm logic technology, which they call their Nexsys Technology, is ramping into production in TSMC's 12 inch Fab 12 in Hsin-Chu, Taiwan. The process offered a MIM capacitor type eDRAM. TSMC shipped 10,000 wafers from the 90 nm process in 2003. This process offers: triple gate oxide, core supply voltage from 1.0V to 1.2V, I/O and analog blocks ranging from 1.8V to 3.3V, multiple threshold voltage (Vt) options for optimized transistor speed and power consumption trade-offs, 50-nanometer gate length for the high speed process, Ni-salicide for better sheet resistance (Rs) in narrow line widths, nine-layer copper interconnect, with an extra redistribution layer optional for flip-chip package, low-k dielectrics with k less than 2.9 for the lowest RC delay and power consumption.[133]

Cell sizes for different technology nodes are shown in the following chart:[133]

<table>
<thead>
<tr>
<th>Technology Node (nm)</th>
<th>1TP*</th>
<th>1TP*</th>
<th>1TP*</th>
<th>1TQ*</th>
<th>1T MIM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell Size (um²)</td>
<td>3.51</td>
<td>1.97</td>
<td>1.0</td>
<td>0.57</td>
<td>0.21</td>
</tr>
</tbody>
</table>

*1T-SRAM developed by MoSys
TSMC 1T eDRAM Capacitors:
TSMC has two embedded DRAM cells in production and a third in development. In 250 nm to 180 nm embedded DRAM products they use a planar DRAM cell (their 1T-P cell developed by MoSys) as shown in the figure below.

Schematic Cross-Section of Planar Capacitor eDRAM Cell [132]

With this cell they run: a 250 nm 4Mb eDRAM networking chip with 81% yield, a 220 nm 2Mb eDRAM networking chip with 86% yield and a 180 nm 10Mb handheld consumer chip with 80% yield. This cell has a sub 10 fF capacitor with multiple bank partitioning which reduces capacitance of the word-lines and bit-lines thereby providing high speed. This cell has no mask adders over the conventional logic process and therefore adds no process cost. [132]

In 130 nm logic technology, TSMC offers a cell with higher capacitance called their 1T-Q cell which was developed by MoSys and is shown below. The cell size in 0.57um2. [132]

Schematic Cross-Section of Shallow Trench Capacitor eDRAM Cell[132]
(MoSys "1T-SRAM-Q")
In 90 nm technology, TSMC is planning to offer a 1T-MIM (metal-insulator-metal) capacitor which they developed themselves. A capacitor-under-bitline architecture is used to reduce the process complexity. The cell size is 0.21 um² and permits integration up to 256-Mb of eDRAM. [132]

![Schematic Cross-Section of a MIM Capacitor eDRAM Cell](image)

### 4.23 UMC

In January of 2003, UMC and MoSys announced that the 1T-SRAM-R (planar capacitor) technology with error correction had been proven in silicon in UMC’s 130 nm logic process. The 1T-SRAM is now available at UMC in 180, 150, and 130 nm technology. [135]

In April of 2004, MoSys and UMC announced silicon validation of the MoSys 1T-SRAM-Q trench embedded memory technology in UMC’s 130 nm logic process. The 1T-SRAM-Q has the folded capacitor cell which is trenched into the STI sidewall. It also has error correction. Typical bit cell size is 0.5 um² for 130 nm technology. The MoSys 1T-SRAM-R planar DRAM technology was verified in UMC’s 130 nm process in January of 2003. [134]

In early 2004, UMC offered 90 nm copper, 130 nm copper, embedded DRAM and mixed signal/RFCMOS processes. [134]

In March of 2005, MoSys announced that Hudson Soft, a manufacturer of game software and entertainment equipment had successfully verified MoSys 1T-SRAM technology in UMC’s 150 nm process. The Hudson Soft Video Game Controller has a 32-bit network CPU and is used in electronic toys made in Japan. [136]
5.0 Summary of eDRAM Cell Types by Supplier/Developer Company

There are many types of eDRAM cells used in making embedded DRAMs. Trench cells include the deep trench which is used in both standalone and embedded DRAMs and the shallow trench which is a simplified structure for eDRAM made in logic-based technology. Stacked cells include the optimized SIS and MIS stacked DRAM cells used in standalone DRAMs and the MIM capacitor cell which is a simplified structure for eDRAM made in logic-based technology. Planar cells are only used for eDRAMs in technologies larger than 130 nm. The following table summarized these cell types by supplier. The type of supplier is color coded.

<table>
<thead>
<tr>
<th>Cells Used for eDRAMs or P-SRAMs</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1. Trench</strong></td>
</tr>
<tr>
<td>a. Deep trench capacitor technology</td>
</tr>
<tr>
<td>(IBM, Infineon, Toshiba, Nanya, Sony, Winbond, SMIC, ProMOS)</td>
</tr>
<tr>
<td>b. Shallow trench technology</td>
</tr>
<tr>
<td>(Fujitsu, Chartered, NEC, TSMC, UMC, Matsushita)</td>
</tr>
<tr>
<td><strong>2. Stacked</strong></td>
</tr>
<tr>
<td>a. Optimized SIS or MIS stacked capacitor</td>
</tr>
<tr>
<td>(Oki, Philips, Powerchip, Renesas, Samsung, Sanyo, Seiko-Epson, SMIC, Elpida, Hynix, Micron)</td>
</tr>
<tr>
<td>b. MIM stacked capacitor (&lt; 90 nm)</td>
</tr>
<tr>
<td>(TSMC, NEC, Renesas, Matsushita, STM)</td>
</tr>
<tr>
<td><strong>3. Planar</strong></td>
</tr>
<tr>
<td>a. (1T-SRAM) (&gt; 180 nm)</td>
</tr>
<tr>
<td>(Dongbu Anam, Kawasaki, LSI-Logic, Agilent, TSMC, UMC, SMIC)</td>
</tr>
</tbody>
</table>

Commodity DRAM suppliers, Logic/ASIC Supplier, IDM, AS-DRAM Supplier
Bibliography


18 Hynix Web Page.
28 IBM Web Page for ASIC Cu-08 process.
29 "IBM and Xilinx prepare for production of first 90nm chips on 300mm wafers", Design and Reuse Headline News, December 16, 2002.


42. P. Clarke, "TigerSHARC moves to IBM's embedded DRAM process", Silicon Strategies, June 17, 2003.


53. TC11IB: 32-bit Microcontroller, Infineon Data Sheet, Revision 2.4, Infineon Web Page, June 2004


55. Inotera Races Ahead With the 300mm Production Ramp-Up -First Volume Production Capacity of 24,000 per month achieved ahead of Schedule, ramp up to more than 50,000 per month by end of 2005, Press Release Infineon and Nanya, October 19, 2004.


68. "NEC Electronics' Embedded DRAM", Hot Technologies, Design Con, 2006 Preview

69. "NEC unveils 0.13-micron embedded DRAM", Electronics News, 27 August 2002


80. Y. Hara, " NEC Electronics to deploy its DRAM in Microsoft's next XBox", EE Times, April 26, 2005.


83. "Philips` Chip Solution Brings Higher Picture Quality to LCD and 100 Hz TV; Loewe to launch new televisions integrating Philips` semiconductor technology", Business Wire, July 1, 2003.

84. B. De Loore, "A video signal processor for motion-compensated field-rate upconversion in consumer television", 24 October 1995 (Philips Research Labs, Hamburg Germany)


87. "SAA4979H; Sample rate converter with embedded high quality dynamic noise reduction and expansion port", Philips Semiconductor Product Information, 2005


90. Renesas Special Feature, Renesas Web Page, May 2005
http://www.renesas.com/jpn/_edge/special03.html


104. B. Neal, "Sony and Toshiba Unveil 65nm eDRAM Process", Ace's Hardware from Silicon Strategies, December 3, 2002


130. Y. Hara, "Toshiba unveils high-density DRAM with floating-body cells", EE Times, February 09, 2005.


141. F. Fishburn, "A highly manufacturable 110 nm eDRAM process with Al2O3 stack MIM capacitor for cost effective high density, high speed, low voltage ASIC memory applications", (Micron), VLSI Technology Symposium, June 2003.


143. S. Wasson, "Details of ATI's Xbox 360 GPU unveiled", The Tech Report, May 19, 2005