Cost-Effective Pipeline FFT/IFFT VLSI Architecture for DVB-H System

Chin-Teng Lin and Yuan-Chu, Yu*
Office of the dean of academic affairs, National Chiao Tung University, Hsinchu, 300, Taiwan, R.O.C.
e-mail: ctilin@mail.nctu.edu.tw
Dept. of Electrical and Control Engineering, Hsinchu, 300, Taiwan, R.O.C.*
e-mail: vincent_yu@emc.com.tw

Abstract — This investigation proposes the novel radix-4² and radix-4⁴ algorithms with the low computational complexities of the radix-16 and radix-64 algorithms but the lower hardware requirement of the radix-4 algorithm. Base on the serial delay feedback path pipeline architecture, the proposed design adopts a multiplierless radix-4 butterfly structure to support 4096-point FFT/IFFT computations. Moreover, the retrenched constant multiplier and eight-folded complex multiplier structures are adopted to decrease the multiplier cost and the coefficient ROM size with the complex conjugate symmetry rule and subexpression elimination technology. The comprehensive comparison results reveal that the proposed R4²SDF design achieves the highest cost efficiency.

I. INTRODUCTION

Future broadband wireless access systems such as wireless LANs (WLAN) and fourth-generation (4G) mobile radio systems require much higher spectral efficiency and service quality than the current standards. The orthogonal frequency division multiplexing (OFDM) modulation scheme not only reduces the receiver complexity but also increases performance on highly dispersive channels. Because of high throughput rate demand by current OFDM systems, such as DVB-H (Digital Video Broadcast in handheld), DAB (Digital Audio Broadcasting), VDSL (Very-high-speed Digital Subscriber Line), and other mobile applications, an efficient FFT processor is required for real-time operations. Because of the increasing demand of handheld consumer products, high throughput, low power and area efficient FFT/IFFT implementation is very worthwhile [2]. Thus, many researches were concentrated on the efficient FFT realization. The pipeline architecture processes regularity, modularity, local connection, and high throughput rate with lower clock frequency [3]. Basically, there are mainly two different pipeline architectures: multipath delay commutator (MDC) architectures [4] and single-path delay feedback (SDF) architectures [4, 5, 6]. The SDF architectures are well known to have a low hardware cost and high cost-efficiency than MDC architectures since the arithmetic operations can be tightly scheduled [4, 5, 6]. He et al. [4] has presented several reliable architectures and the detailed comparisons of the corresponding hardware cost for efficient pipeline FFT processors. The comparison results of these architectures indicate that the R2²SDF has the highest butterfly utilization and lowest hardware resource usage following with the high efficient feedback memory architecture. However, the radix-2² algorithm has a higher multiplicative complexity than the high-radix FFT algorithms. In this study, we proposed two high cost effective 4096-point pipeline FFT/IFFT processors for DVB-H system, namely R4²SDF and R4³SDF design, to achieve the less complex multiplicative complexities as radix-16 and radix-64 based algorithm with only radix-4 based algorithm. Results of comprehensive comparison further indicate that the proposed R4²SDF and R4³SDF based pipeline processor achieve a higher utilization with a smaller hardware requirement than R2²SDF-based pipeline processor [4][5] in the 4096-point FFT/IFFT computation, and thus have higher cost efficiency. Thus, the proposed design is very appropriate for SoCs IP in DVB-H system. The remainder of this study is structured as follows. A new R4²SDF and R4³SDF FFT/IFFT algorithms are given in Section II. Section III demonstrates the proposed R4²SDF and R4³SDF VLSI architectures. Section IV tabulates the comparison results in terms of hardware utilization and cost to demonstrate the high cost-efficiency of the proposed architectures. The final section draws conclusions.

II. NEW RADIX-4² AND RADIX-4⁴ BASED FFT/IFFT ALGORITHM

A. Radix-4² based FFT/IFFT Formula

The FFT of the N-point input x[n] is given by

\[ X[k] = \sum_{n=0}^{N-1} x[n] \cdot W_n^k, \]

where \( W_N = e^{-j2\pi / N} \). Applying a 3-dimensional linear index map,

\[ n = \frac{N}{4} n_1 + \frac{N}{16} n_2 + n_3, \quad k = k_1 + 4k_2 + 16k_3. \]

The common factor algorithm (CFA) [7] form can be written as

\[ X[k_1 + 4k_2 + 16k_3] \]

1 This work was supported in part by the National Science Council of Taiwan Grant NSC93-2218-E-009-061.
where the butterfly structure of the first stage takes the form

\[ b^k_N \left( \frac{N}{16} x_{n_2 + n_3} + \frac{N}{4} \right) + \left( -1 \right)^k x \left( \frac{N}{16} x_{n_2 + n_3} + \frac{3N}{4} \right), \quad (4) \]

Following a similar decomposition procedure, Eq. (3) can be decomposed as

\[ x[k_1 + 4k_2 + 16k_3] = \frac{N}{16} \sum_{n_k=0}^{N-1} b^k_N \left( \frac{N}{16} n_k + \frac{N}{4} \right) \left( N \right) W^{\eta n_k}, \quad (5) \]

Meanwhile, the butterfly structure of the second stage can be obtained as

\[ b^k_N \left( \frac{N}{16} n_k + \frac{N}{4} \right) + \frac{N}{4} \left( 1 \right)^{k} b^k_N \left( \frac{N}{16} n_k + \frac{N}{4} \right) \]

\[ + W^{2k_{321321}} \left( -1 \right)^k b^k_N \left( \frac{N}{16} n_k + \frac{N}{4} \right) \left( 1 \right)^{k} b^k_N \left( \frac{N}{16} n_k + \frac{N}{4} \right), \quad (6) \]

The second radix-4 butterfly structure in (6) is the same as the first radix-4 butterfly structure in (4) after simplification of the common factor of the constant multiplier. The detailed hardware structure of constant multiplier is described in the next section. The complete radix-4² DIF FFT algorithm is obtained by applying the CFA procedure recursively to the remaining FFTs of length N/16 in (5). The radix-4² algorithm has the same multiplicative complexity as the radix-16 algorithm, but still retains the radix-4 butterfly structure. Significantly, the radix-16 algorithm clearly has a lower multiplicative complexity than other low-radix algorithms, such as a radix-2² algorithm. Following with the similar decomposition procedure, the radix-4² DIF IFFT computation could be obtained by the similar radix-4 butterfly structure with only some sign inversions.

B. Radix-4³ based FFT/IFFT Formula

Applying another 4-dimensional linear index map in (1),

\[ n = \frac{N}{4} n_1 + \frac{N}{16} n_2 + \frac{N}{64} n_3 + n_4, \]

\[ k = k_1 + 4k_2 + 16k_3 + 64k_4. \]

The common factor algorithm (CFA) [7] form can be written as

\[ X[k_1 + 4k_2 + 16k_3 + 64k_4] = \frac{N}{64} \sum_{n_k=0}^{N-1} b^k_N \left( \frac{N}{64} n_k + \frac{N}{64} \right) W^{\eta n_k}, \quad (7) \]

\[ + W^{2k_{321321}} \left( -1 \right)^k b^k_N \left( \frac{N}{64} n_k + \frac{N}{64} \right) + W^{3k_{321321}} \left( j \right)^k b^k_N \left( \frac{N}{64} n_k + \frac{N}{64} \right), \quad \]

\[ + W^{2k_{321321}} \left( -1 \right)^k b^k_N \left( \frac{N}{64} n_k + \frac{N}{64} \right) + W^{3k_{321321}} \left( j \right)^k b^k_N \left( \frac{N}{64} n_k + \frac{N}{64} \right) + W^{2k_{321321}} \left( j \right)^k b^k_N \left( \frac{N}{64} n_k + \frac{N}{64} \right), \quad (9) \]

The complete radix-4³ DIF FFT algorithm is obtained by applying the CFA procedure recursively to the remaining FFTs of length N/64 in (8). Thus, the radix-4³ algorithm has few multiplicative complexities as the radix-64 algorithm, but still retains the simple radix-4 butterfly structure. For example, the numbers of complex multiplications in the 4096-point FFT computation adopting the radix-2², radix-4² and radix-4³ algorithms are 13996, 7425 and 3969, respectively. Thus, the proposed radix-4³ algorithm has a lower multiplicative complexity (71.6%) than the radix-2² algorithm [4][5]. Significantly, the radix-64 algorithm clearly has a lower multiplicative complexity than the proposed radix-4³ algorithm and other low-radix algorithms. According to the similar radix-4 based butterfly architecture with only some sign inversions, the radix-4³ DIF IFFT computation could be obtained.
III. PIPELINE 4096-POINT R4\textsuperscript{2}SDF AND R4\textsuperscript{3}SDF BASED FFT/IFFT VLSI ARCHITECTURE

Based on the new proposed radix-4\textsuperscript{2} and radix-4\textsuperscript{3} DIF FFT algorithms, the novel radix-4\textsuperscript{2} single-path delay feedback (R4\textsuperscript{2}SDF) and radix-4\textsuperscript{3} single-path delay feedback (R4\textsuperscript{3}SDF) architectures for supporting the 4096-point FFT/IFFT computations were shown in Fig.1 and 2, respectively. Two proposed architectures both require six butterfly stages with 4095-word shift registers. The R4\textsuperscript{2}SDF based 4096-point FFT/IFFT pipeline processor requires three constant multipliers and two complex multipliers. And, the R4\textsuperscript{3}SDF based 4096-point FFT/IFFT pipeline processor requires four constant multipliers and one complex multipliers. The detailed operations of each element are described as follows.

![Fig. 1. Block diagram of the R4\textsuperscript{2}SDF-based 4096-point FFT/IFFT VLSI architecture.](image1)

![Fig. 2. Block diagram of the R4\textsuperscript{3}SDF-based 4096-point FFT/IFFT VLSI architecture.](image2)

![Fig. 3. Block diagram of the radix-4 butterfly architecture.](image3)

![Fig. 4. The proposed 4 operational modes in the radix-4 based butterfly blocks.](image4)

![Fig. 4. The timing sequences of 4 operation modes in the proposed pipeline architecture.](image5)

A. Radix-4 Butterfly

The derivation results of the radix-4\textsuperscript{2} and radix-4\textsuperscript{3} algorithms reveal that both the FFT/IFFT butterfly computation in (3) and (8), can be easily completed with the same radix-4 butterfly architecture. Notably, the radix-4 butterfly structure only requires trivial multiplication, which involves real-imaginary swapping and sign inversion, and which does not require any complex multiplication. Figure 3 illustrates the proposed radix-4 butterfly structure, which only includes four four-input complex adders. The radix-4 based butterfly structure is more cost-efficient than higher-radix-based butterfly structures. Moreover, the proposed radix-4\textsuperscript{2} algorithm has the same complex multiplication complexity as the radix-16 algorithm, and radix-4\textsuperscript{3} algorithm further has the few complex multiplication complexity as the radix-64 algorithm. Thus, the proposed two pipeline architectures have the high cost efficiency of lower radix architectures.

B. Memory Structure

The memory structure of butterfly stage is well known to be an important issue for the high cost-effective FFT/IFFT pipeline processor design. In this study, the delay feedback based memory structure is adopted. In order to compute the radix-4 based butterfly computations, the input data and the intermediate results have to be reordered as four concurrently data streams using memory as shown in Fig. 3. Figure 4(a) shows the four proposed operation modes of the radix-4 butterfly stage to finish the data reordering and the butterfly computation. Operation modes 0–2 are adopted in the data reordering, and operation mechanisms 3 are adopted in the FFT/IFFT computation. Each radix-4 butterfly unit applies the three parallel memories to store the serial data input and butterfly output in the feedback paths as presented in Fig. 4(a). The timing sequence of N-point FFT computation can be divided into four stages, each containing N/4 clock cycles as presented in Fig. 4(b). The required number of memory cells for the kth stage is 3 \(N/(4^k)\). Significantly, the SDF based pipeline FFT/IFFT structure is highly regular, which has the high effective memory structure with the simpler routing complexity [4, 5, 6].

C. Constant Multiplier

Based on the derivation results in Section II, the radix-4\textsuperscript{2} algorithm requires some complex multiplications, namely \(w_{16}^{2k}, w_{16}^{4k}\), and \(w_{16}^{3k}\) in the 4096-point FFT/IFFT computation in (6). According to the SDF based architecture as depicted in Fig. 1, a single data stream passes through the constant multipliers and complex multipliers. There is only one complex multiplication was computed in (6) during each cycle. Then, the three full complex multipliers can be simplified as a single constant multiplier. This subsection follows three steps to reduce the complex multipliers to the most economical constant multipliers in the radix-4\textsuperscript{2} and radix-4\textsuperscript{3} architecture. The implementation of constant multiplier in the radix-4\textsuperscript{2} architecture was presented as
below. First, the multiplication of twiddle factors from Eq. (6) is realized as the constant multiplier, which only contains shifters and adders as shown in Fig. 5. Second, the complex conjugate symmetry rule is applied to decrease the number of complex multiplications to only two constant multiplications per stage with some shuffle circuits as shown in Fig. 6, thus achieving a constant multiplier cost reduction of 83%. Finally, the subexpression elimination algorithm [8] is adopted to reduce the number of shift circuits by more than 20%, and the number of complex adders by 50% in the one constant multiplier, as depicted in Fig. 5. The strictest constant multipliers are obtained in the proposed architectures by following these three steps. The cost penalty of the constant multiplier is thus minimized. Similarity, the radix-4 algorithm has two retrenched constant multipliers as depicted in (9). The constant multiplier of second stage in R4’s SDF design is the same as the constant multiplier in R4’s SDF design. Following the similar reduction steps, the constant multiplier of the third stage increases slightly control complexity than the constant multiplier in second stage.

**D. Eight-Folded Complex Multiplier**

The proposed 4096-point R4’s SDF design has one complex multiplier and one coefficient ROM to realize the complex multiplication of twiddle factors $W_n^{n_k}e^{j\frac{a_k}{4}+j\frac{b_k}{4}}$ in (8). However, the proposed 4096-point R4’s SDF design requires two complex multipliers and two coefficient ROMs to realize the $W_n^{n_k} e^{j\frac{a_k}{4}}$ in (4). To decrease the ROM size, the complex conjugate symmetric rule and subexpression elimination [8] are applied to devise one eight-folded complex multiplier as shown in Fig. 5. The proposed eight-folded complex multiplier could reduce the coefficient ROM size of 87.5%. The R4’s SDF and R4’s SDF design only have to store 32 and 512 words in the coefficient ROM, respectively. Although, the R4’s SDF design requires the less ROM size than R4’s SDF design, two complex multipliers and two coefficient ROMs were required to complete the 4096-point FFT/IFFT computation in the R4’s SDF based architecture. The ROM address and data control circuit are shown in Table I.

![Fig. 6. The block diagram of eight-folded algorithm in the coefficient ROM.](image)

**IV. COMPARISON RESULTS**

This section presents the comprehensive comparison results of several famous pipeline FFT/IFFT architectures to demonstrate the high cost-efficiency of the proposed R4’s SDF and R4’s SDF FFT/IFFT architectures. The architectures were compared in two indices, namely cost and utilization, to express the cost efficient of the proposed FFT/IFFT architecture, as listed in Tables II and III. Table II lists the required hardware resources, where $T$ denotes the number of complex adders required in the implementation of the constant multiplier. Significantly, the area of the complex multiplier is known to be the dominant cost index in the pipeline FFT/IFFT design. The comparison results in Table II clearly demonstrate that the proposed R4’s SDF based-FFT/IFFT architecture has the fewest complex multipliers requirement among other pipeline architectures. The 4096-point R4’s SDF based FFT/IFFT architecture only needs one complex multiplier, which is 83% and 95% below the requirement of the R2’s SDF and R8MDC FFT/IFFT architectures, respectively. Additionally, the proposed architecture maintains the minimum shift registers requirement. Although the proposed R4’s SDF and R4’s SDF based architecture needs slightly more complex adders than the R2’s SDF based architecture, this small cost penalty is acceptable. To estimate the total chip cost in the 4096-point
FFT/IFFT architectures, which includes the number of complex multipliers, complex adders and memory size, the conventional comparative methodology [5][9] with the unit of equivalent adders was used to estimate the cost value between the different architectures. Based on the implementation results in our process, we convert the area of each complex multiplier and complex memory to the 50 and 1.3 complex adder, respectively, and the scheme with three real multiplications and five real additions, in the implementation. The rightmost column of Table II lists the area indexes of the equivalent adder of the 4096-point FFT/IFFT architecture. Clearly, the proposed R4 SDF-based 4096-point FFT/IFFT architecture has the lowest hardware requirements. Significantly, the cost advantage of our proposed architecture becomes more evident when the transform length is larger. Thus, the proposed R4 SDF architectures have lower hardware cost than R4 SDF and other famous pipeline FFT/IFFT architecture in terms of the number of ROMs, complex multipliers, complex adders, constant multipliers and shift registers.

**Table II**

<table>
<thead>
<tr>
<th>Pipeline architecture</th>
<th>Utilization rate of complex Mult.</th>
<th>Utilization rate of complex adders (including constant mult.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R2SDF</td>
<td>50%</td>
<td>50%</td>
</tr>
<tr>
<td>R4SDF</td>
<td>75%</td>
<td>75%</td>
</tr>
<tr>
<td>R8SDF</td>
<td>87.5%</td>
<td>87.5%</td>
</tr>
<tr>
<td>R2 SDF</td>
<td>75%</td>
<td>75%</td>
</tr>
<tr>
<td>R4 SDF</td>
<td>87.5%</td>
<td>87.5%</td>
</tr>
<tr>
<td>R2MDC</td>
<td>62.5%</td>
<td>50%</td>
</tr>
<tr>
<td>R4MDC</td>
<td>75%</td>
<td>75%</td>
</tr>
<tr>
<td>R2 SDF</td>
<td>87.5%</td>
<td>87.5%</td>
</tr>
<tr>
<td>R4 SDF</td>
<td>87.5%</td>
<td>87.5%</td>
</tr>
<tr>
<td>Proposed R4 SDF</td>
<td>96.9%</td>
<td>96.9%</td>
</tr>
</tbody>
</table>

Table III shows the comprehensive comparison of the hardware utilization rate in terms of the utilization rate of complex multipliers, complex adders and complex memory. Clearly, the proposed R4 SDF architecture achieves the highest complex multiplier utilization rate among pipeline architecture (96.9%). Additionally, the proposed architecture maintains the maximum complex memory utilization rate of 100%. Furthermore, the proposed R4 SDF architecture, including the constant multipliers, has the highest complex adder utilization rate of 60.42%. Thus, the purposed R4 SDF architecture achieves a higher hardware utilization rate than R4 SDF and other well-known pipeline FFT/IFFT architecture in terms of the utilization rate of complex multipliers, complex adders, constant multipliers and complex memory.

**V. CONCLUSION**

This investigation develops two high cost effective R4 SDF and R4 SDF serial pipeline VLSI architectures that support the 4096-point FFT/IFFT computations. The proposed R4 SDF pipeline FFT/IFFT architecture has lower multiplicative complexity and higher hardware utilization rate with smaller cost than R4 SDF and other pipeline architectures. Thus, these features ensure that the proposed R4 SDF pipeline 4096-points FFT/IFFT processor design is certainly amenable to the DVB-H system.

**ACKNOWLEDGMENT**

The authors would like to thank the National Science Council of the Republic of China, Taiwan for financially supporting this research under Contract No. (NSC NSC93-2218-E-009-061). Also, the authors would like to thank anonymous referees for their valuable suggestions to this paper.

**REFERENCES**


