Tunable Delay Element for Low Power VLSI Circuit Design

Jung-Lin Yang, Chih-Wei Chao, and Sung-Min Lin
Institute of Electronic Engineering
Southern Taiwan University of Technology
Yongkang City, Tainan County 71005, Taiwan (R.O.C.)
jayang@mail.stut.edu.tw, {m9430106, m9235214}@webmail.stut.edu.tw

Abstract—We proposed a low-power tunable delay element with several nice features. Initially, we develop this matched delay element for implementing self-timed datapath components. Surprisingly, we found this design is also suitable for many high performance applications with low power requirement after examining its circuit characteristics in more detail. Tunable and asymmetric characteristics are the two major concerns of this delay line circuit. Besides, the circuit itself also demonstrates valuable characteristics such as well adjustment to the operating temperature disparity on the delay and the technology variation-tolerant nature. In order to keep the low power intuition of utilizing asynchronous circuits, we spend a huge effort to cut down the overall power consumption. The proposed tunable delay element consumes less average power than a 4-stage minimum size inverter chain. A 4 ns and 8 ns delay implemented by our design needs only 26μW and 30μW respectively for the TSMC 0.35μm technology. To the best of our knowledge, this is the lowest power consumption of the programmable delay element of the same kind so far.

I. INTRODUCTION

There are many applications using delay elements for example the delay-locked loops (DLLs), digitally control oscillators (DCOs), self-timed circuits, multi-clock domains synchronization, local timing generator, and so on. When we design a delay element for different applications, we would like to know the insensitivity to temperature and process variation for a specific delay circuit. In some occasion, we would like the delay circuit to be high power consumption and low EMI. In the discussion, we focus on the usage as matched-delay elements in the self-timed systems or the asynchronous circuits. Therefore, power, area, and controllability are the key issues of this paper.

A. Inverter Chain

Inverter chain is a simple way to generate delay time. It is advantageous over wide environmental and process variation; and it keeps a steady static-state power dissipation and better signal integrity. The drawback of the delay element is the inverter chain is area-expensive and variant to swing voltages.

B. Transmission Gate

Transmission gate delay element (TDE) uses channel resistor of transistor to control charging/discharging time with NMOS capacitor. The advantage of transmission gate architecture provides low power consumption in its relay feature. The disadvantage is when there is a need for fast switching between on and off, it will consume large amount of power since the load capacitance is fully charged and discharged. Also, signal integrity of this design is poor due to the resistance on the delay path. The problem may be overcome by using Schmitt triggering circuitry; however, it may exhaust more power [1].

C. Shunt Capacitor-based

This type of delay element uses Shunt capacitor [2]. Bazes uses voltage source to control the delay time of the proposed delay element. For the purpose of reducing length of NMOS resistor, he uses another NMOS device to form a capacitor. For the equivalent RC delay time, this design reduces the size of area. This method made suffer from high power consumption that is caused from shunt capacitor.

D. Current-starved Based

Current-starved-based delay element controls the delay time by manipulating charge/dischARGE current. There are two common techniques to control current in the delay line: altering the W/L ratio of the transistor sizes; and controlling the gate-source voltage on the transistors. There are three types of basic current-starved delay elements [3]. The advantages of the current-starved delay element is it may have the longer delay time to and have a better performance in the static power consumption by using the current source to generate a bias voltage.

E. Thyristor Based

A Thyristor-based delay element is similar to current-starved, which uses the current mirror to adjust delay time [4]. This type of delay element adjusts the pull-up/pull-down path by altering length of the transistors in order to control the delay time. While the delay time is controlled by changing the transistor size by increasing the parasitic capacitance, this approach will lead to extra power consumption. Thyristor-based delay element is capable of generating a much longer delay time than the previous types. Also, it is insensitive to temperature and voltage variation. The adoption of positive feedback technique also improves signal integrity, but when delay time increases, the signal integrity gets worse. Another disadvantage of the Thyristor-based delay element is its area overhead.

II. PROPOSED TUNABLE DELAY ELEMENT

As we mentioned in the introduction, delay elements play very important role in many applications. A specific example, self-timed circuits, draws us more attention than the others. Two essential properties, being adjustable and asymmetric, are very crucial for being a matched delay when building the self-timed bundled-data component. Thus, we proposed a tunable delay element with extreme low power feature in this
work. However, this asymmetric delay element is not limited to self-timed applications only.

A. Implementation

The proposed tunable delay element consists three parts: delay adjuster, controllable delay line, and fast-reset driver (see Fig. 1). The delay adjuster controls the delay time of the target transition edge. The controllable delay line forms a delay function based on the delay adjuster’s signal transition slope. And, the fast-reset driver pulls down the output rapidly and sharpens the signal transition back to the regular transient slope and voltage level.

B. Delay Adjuster

The delay adjuster is a simple inverter with controllable pulled-down circuitry, a diode-connected NMOS device (Mn3) and a NMOS resister (Mn2). The diode-connected transistors are used in many places within our design to reduce the signal transition swing, which is the key factor making our delay element extreme low power. The NMOS resistor controls discharging current by altering Mn2’s channel length.

C. Controllable Delay Line

The basic idea of our delay line is to make use of stretched transient delay caused by flattened signal transition. It would be best to demonstrate this influence by examining the waveform shown in Fig. 2. Line S1 and S2 reveal the reduced swing property of the internal signals. In addition to this, the smoothly rising and falling transitions of the line S2 and S1 induce the needed long delay. However, if we did not control the charging/discharging currents properly, the short circuit current will become a disaster in term of power consumption. Thus, we also use diode-connected device (Mp2 and Mp4) to trim down the operating current of the delay line.

D. Fast-reset Driver

In order to postpone one signal transition edge but not the other, a fast-reset driver can be used. This driver does not only provide large driving capability to its output but also making pulled-down transition hastily. Besides these two major tasks, it is also responsible for restoring the reduced voltage swing of the internal transition to the regular voltage level. We should notice that it is impossible to drive the output properly without Mn6. Mn6 is a rapid cut-off device controlled by the input signal to co-operate with the fast-reset driver. It stops the postponed falling edge from propagating to the output and restores the S3 signal to the supply voltage level.

III. DELAY ELEMENT PROPERTY ANALYSIS

In this section, we would like to exam the proposed tunable delay element by its post-layout SPICE simulation. We carefully draw a delay element template with preserved vast space for varying the delay adjuster. The layout is shown in Fig. 3. TSMC 0.35 μm technology is used to exam all characters discussed in the following section.

A. Delay Time Calibration

Fig. 4 is the delay function of varying Mn2’s channel length with fixed width of 0.4 μm. We swept the length from the 0.35 μm to 12.6 μm to calibrate a delay time look-up table in the range of 2.7 ns to 11.1 ns. The transient delay of the rising edge is roughly 300 ps and 150 ps for the falling edge to drive a typical FO4 loading. The simulation results also confirm that the postponed internal edges are filtered out by the fast-reset driver. For the simplicity, we directly change the length of the Mn2 from the template’s layout to obtain the desired delays. Actually, we could utilize the similar technique presented in [5] to form a more flexible programmable delay element when necessary.

B. Extreme Low Power

The significant contribution of this work is the extreme low power nature of the proposed delay element. We compare our work to the two existing delay elements, CMOS thyristor-based and current-starved delay element. As we can see from the Table I, the improvement is remarkable. We have no definite transistor sizing information on the first one. Thus, we use the numbers appear in [4] directly. Based on our best knowledge of transistor sizing techniques, we re-implement the current-starved delay element using the same technology for the comparison.

In additions, we also implement a 4-stage minimum size inverter chain to extract reasonable lower-bound power consumption for a circuit structure similar to ours. Using the same TSMC 0.35 μm technology, the inverter chain consumes roughly 24 μW, which is very close to our delay element. It is evidently to note that there is not much we can do to further attempt on saving the power on the post-layout simulation result.
C. Well Adapting to Operating Temperature

Another issue that we would like to address here is how well this delay element reacts to the temperature variations. We know that CMOS digital circuits are very sensitive to their operating temperatures. Thus, a practical delay element for the purpose of matching the worst-case evaluation delay must have the similar influence of temperature on delay to the target circuits. For the target circuits, we chains 22 and 42 4-input NAND gates to construct the 4 ns and 8 ns delay of the dummy testing circuits. Referring to the calibrated look-up table, we choose 2.45 \( \mu m \) and 8.4 \( \mu m \) as the length of \( M_{n2} \) to match the delay of the target circuits. Then, all circuits are simulated by altering the temperature range from 25 to 125 \( ^\circ C \). In Fig. 5, we can see that our tunable delay element has better delay variation matching character for the longer delay. Although the 4 ns one is a bit shorter than what we wanted, the difference is still within the 10% safety margin in very high temperature. Both cases show nearly identical delay variation tendency as their target circuits that serves as evidence of well-adaptive circuit quality to operating temperatures.

D. Technology Variation Tolerant

The last characteristic examined here is the influence of channel length variation on delay. Technology variation is unavoidable for today’s CMOS fabrication technologies. Thus, there are no two transistors the same when they are produced on silicon. What we get from fabricated chips may not be 100% matched to what we have drawn in the layout. Thus, we add/subtract \( \frac{1}{4} \lambda \) (\( \lambda = \frac{1}{2} \) min. length) to the \( M_{n2} \)’s drawing length to mimic the uncontrollable channel length variations. We learn from the Fig. 6 that the delay variation is ranging from -107 to +94 ps. For the two specific designs, 4 ns and 8 ns, the variations are (-40, +83) ps and (-76, +64) ps accordingly. These delay variations are far below the acceptable offset that can be easily overcome by the added safety margin. These results lead to the conclusion that our tunable delay element is a technology variation-tolerant design.

IV. Conclusion

We have obtained a tunable delay element implementation with a predominant attribute on low operating power, asymmetrical characteristic, and programmability, which is suitable for high-performance design such as self-timed circuit. This tunable design shows less power consumption than the 4-stage inverter chain using the minimum size gate width. As we program our design to 4 ns and 8 ns delay, it shows only 26 \( \mu W \) and 30 \( \mu W \) respectively by using the TSMC 0.35 \( \mu m \) technology; this is the best tunable delay element as compared to similar designs of such kind.
REFERENCES


